



### CST4485 P-Ch 40V Fast Switching MOSFETs

- ★ 100% EAS Guaranteed
- ★ Green Device Available
- ★ Super Low Gate Charge
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology

#### CST4485 Product Summary



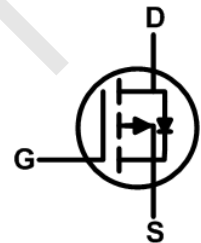
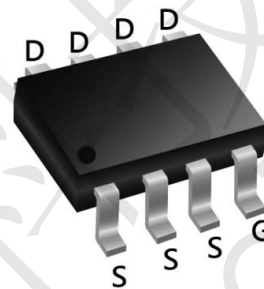
BVDSS	RDSON	ID
-40V	14 mΩ	-13 A

#### CST4485 General Description

The CST4485 is the high cell density trenched P-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

The CST4485 meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

#### CST4485 SOP8 Pin Configuration



#### CST4485 Absolute Maximum Ratings (TA= 25°C, unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V <sub>DS</sub>	-40	V
Gate-Source Voltage	V <sub>GS</sub>	±20	V
Continuous Drain Current	I <sub>D</sub>	TA=25°C	-13
		TA=100°C	-8.5
Pulsed Drain Current <sup>1</sup>	I <sub>DM</sub>	-52	A
Single Pulse Avalanche Energy <sup>2</sup>	EAS	80	mJ
Total Power Dissipation	P <sub>D</sub>	3	W
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to 150	°C

#### CST4485 Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction-to-Ambient <sup>3</sup>	R <sub>θJA</sub>	41	°C/W



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#### CST4485 Electrical Characteristics ( $T_J = 25^\circ\text{C}$ , unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
<b>Static Characteristics</b>							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-40	-	-	V	
Gate-body Leakage current	$I_{GSS}$	$V_{DS} = 0V, V_{GS} = \pm 20V$	-	-	$\pm 100$	nA	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -40V, V_{GS} = 0V$	$T_J = 25^\circ\text{C}$	-	-	-1	$\mu A$
			$T_J = 100^\circ\text{C}$	-	-	-100	
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-1.0	-1.5	-2.2	V	
Drain-Source On-Resistance <sup>4</sup>	$R_{DS(on)}$	$V_{GS} = -10V, I_D = -10A$	-	14.0	19	m $\Omega$	
		$V_{GS} = -4.5V, I_D = -5 A$	-	19.5	25		
Forward Transconductance <sup>4</sup>	$g_{fs}$	$V_{DS} = -10V, I_D = -10A$	-	44	-	S	
<b>Dynamic Characteristics<sup>5</sup></b>							
Input Capacitance	$C_{iss}$	$V_{DS} = -20V, V_{GS} = 0V, f = 1\text{MHz}$	-	2525	-	pF	
Output Capacitance	$C_{oss}$		-	190	-		
Reverse Transfer Capacitance	$C_{rss}$		-	172	-		
Gate Resistance	$R_g$	$f = 1\text{MHz}$	-	10	-	$\Omega$	
<b>Switching Characteristics<sup>5</sup></b>							
Total Gate Charge	$Q_g$	$V_{GS} = -10V, V_{DS} = -20V, I_D = -10A$	-	35	-	nC	
Gate-Source Charge	$Q_{gs}$		-	5.5	-		
Gate-Drain Charge	$Q_{gd}$		-	8	-		
Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = -10V, V_{DD} = -20V, R_G = 3\Omega, I_D = -10A$	-	14.5	-	ns	
Rise Time	$t_r$		-	20.2	-		
Turn-Off Delay Time	$t_{d(off)}$		-	32	-		
Fall Time	$t_f$		-	10	-		
<b>Drain-Source Body Diode Characteristics</b>							
Diode Forward Voltage <sup>4</sup>	$V_{SD}$	$I_S = -10A, V_{GS} = 0V$	-	-	-1.2	V	
Continuous Source Current	$I_S$	$T_C = 25^\circ\text{C}$	-	-	-13	A	

Note :

1. Repetitive rating, pulse width limited by junction temperature  $T_{J(MAX)} = 150^\circ\text{C}$ .
2. The EAS data shows Max. rating . The test condition is  $V_{DD} = -25V, V_{GS} = -10V, L = 0.1\text{mH}, I_{AS} = -34A$ .
3. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 20Z copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$ .
5. This value is guaranteed by design hence it is not included in the production test.



#### CST4485 Typical Characteristics

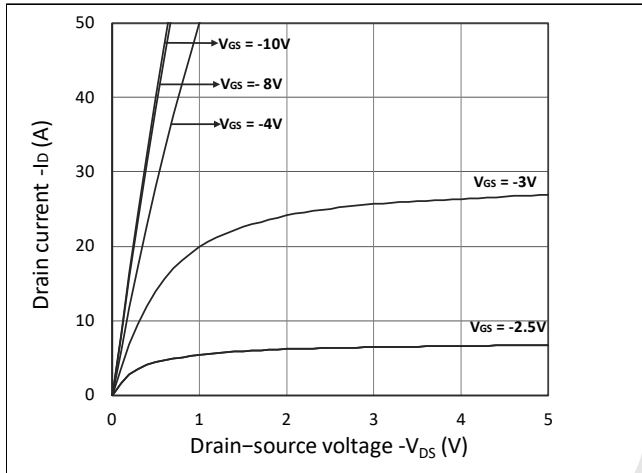


Figure 1. Output Characteristics

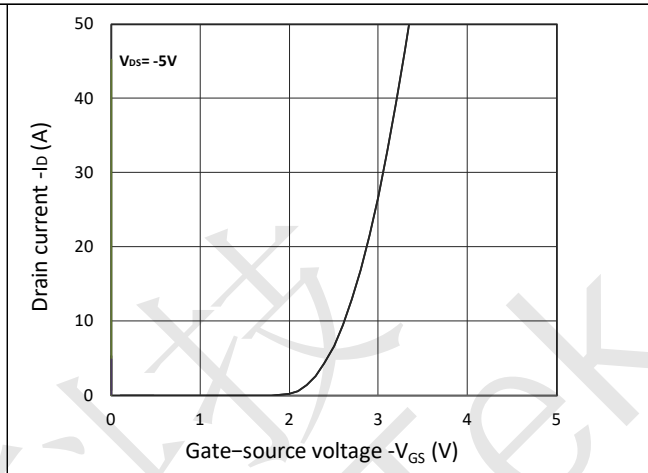


Figure 2. Transfer Characteristics

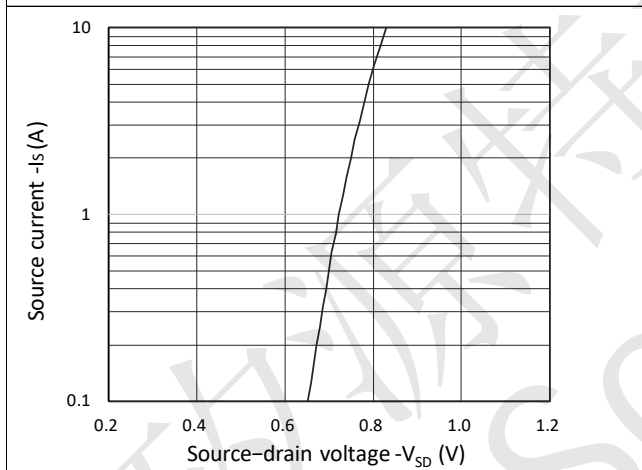


Figure 3. Forward Characteristics of Reverse

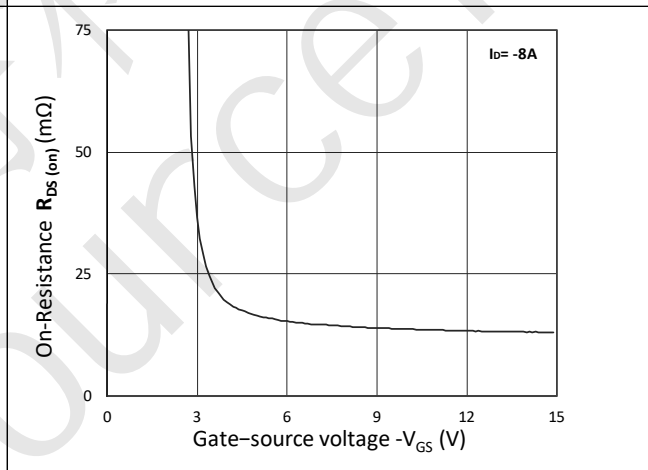


Figure 4.  $R_{DS(on)}$  vs.  $V_{GS}$

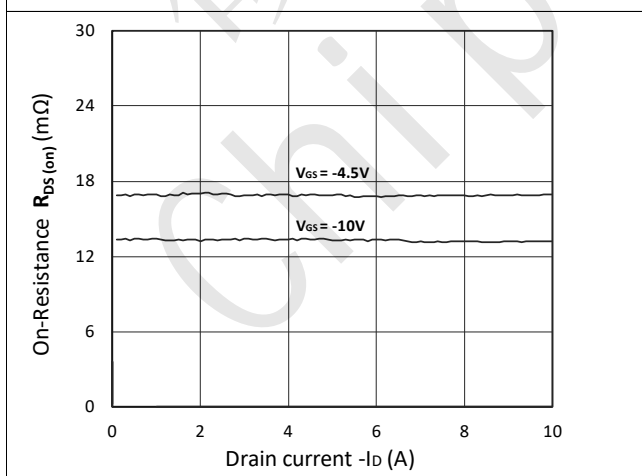


Figure 5.  $R_{DS(on)}$  vs.  $I_D$

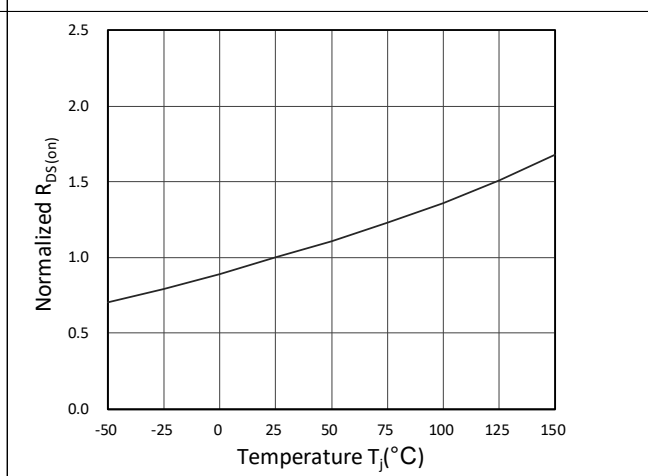


Figure 6. Normalized  $R_{DS(on)}$  vs. Temperature



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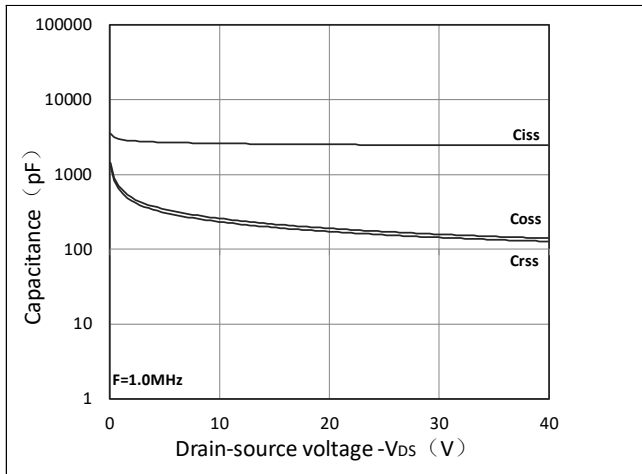


Figure 7. Capacitance Characteristics

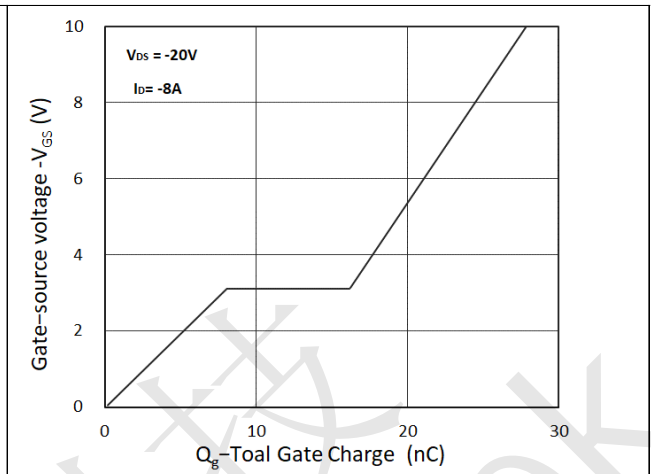


Figure 8. Gate Charge Characteristics

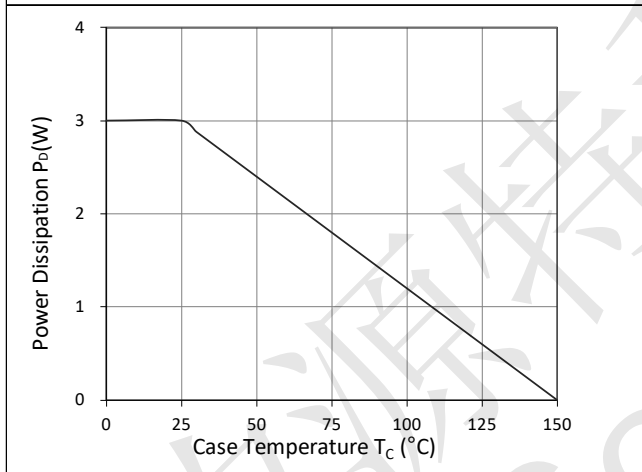


Figure 9. Power Dissipation

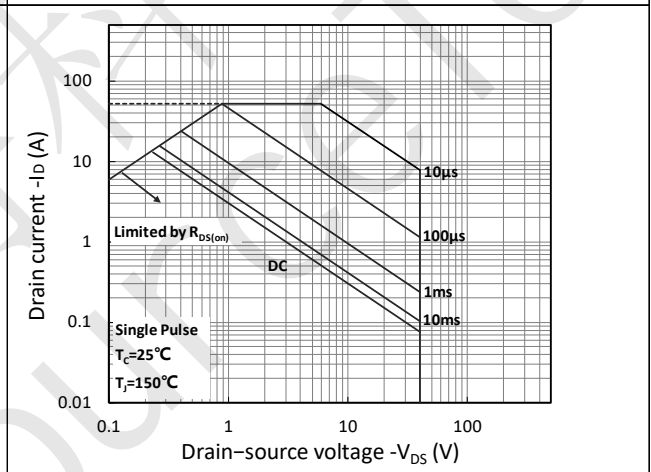


Figure 10. Safe Operating Area

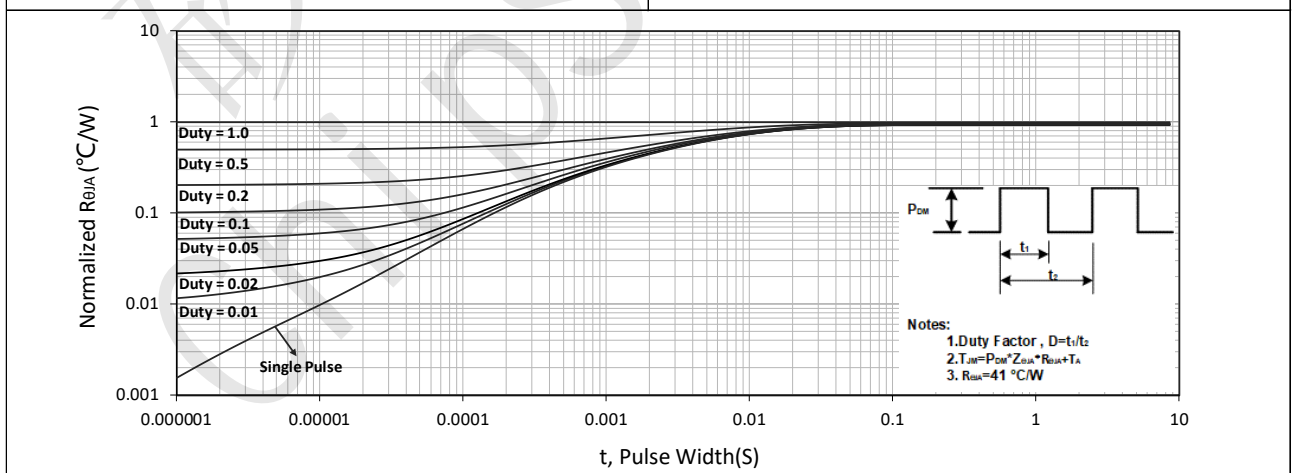
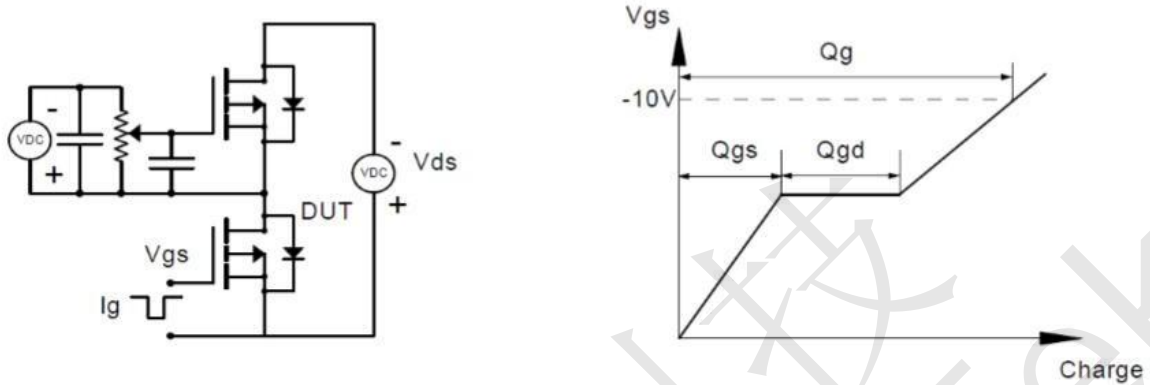


Figure 11. Normalized Maximum Transient Thermal Impedance

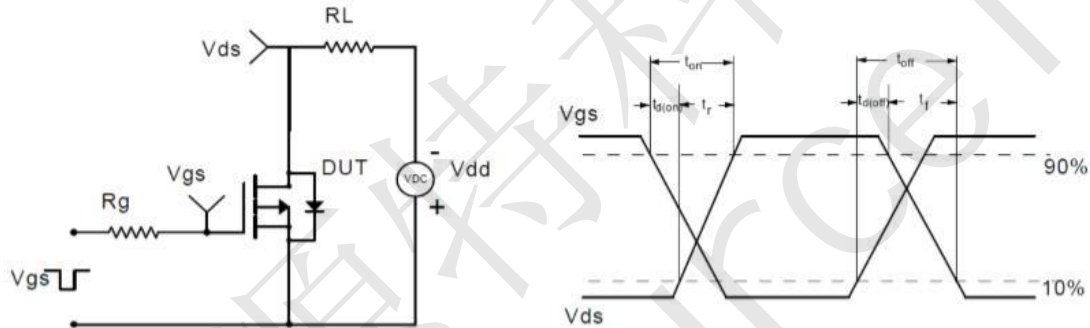


#### CST4485 Test Circuit

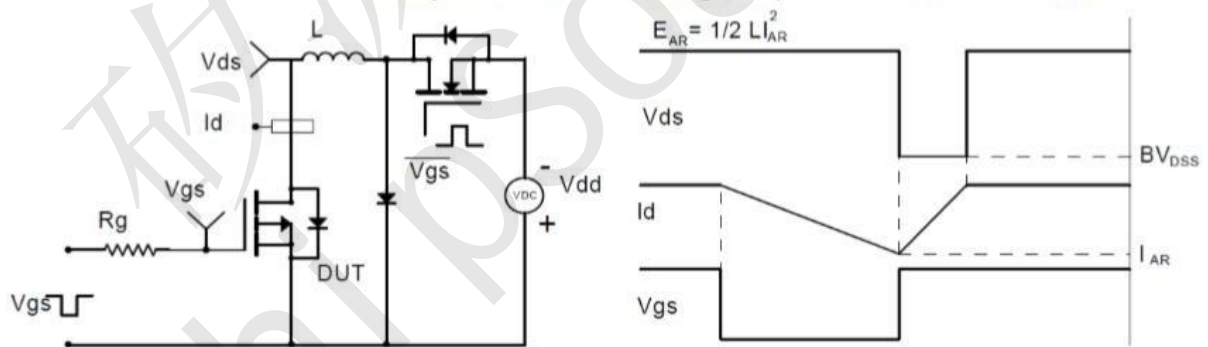
##### Gate Charge Test Circuit & Waveform



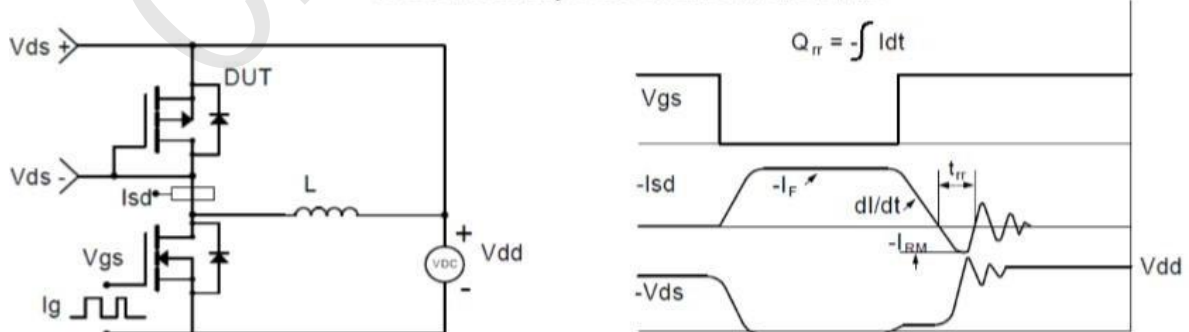
##### Resistive Switching Test Circuit & Waveforms



##### Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

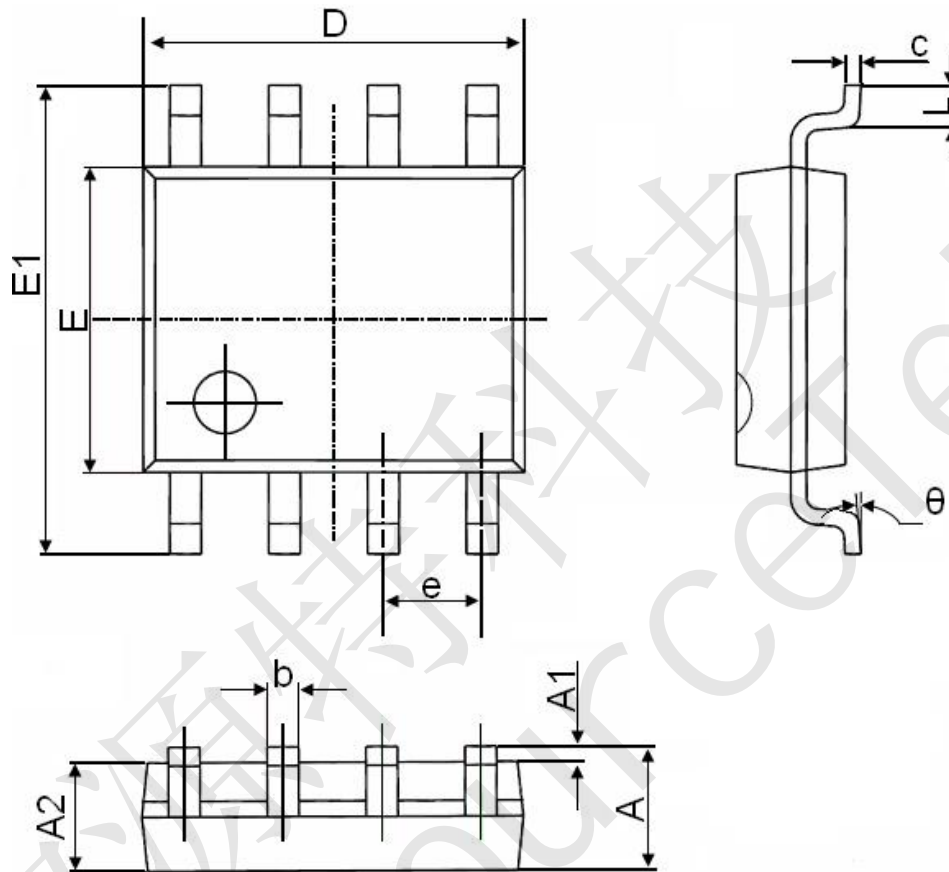


##### Diode Recovery Test Circuit & Waveforms





#### CST4485 SOP-8 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°