P-Channel Enhancement Mode Power MOSFET **MXN3349**

DESCRIPTION

The MXN3349 uses advanced trench technology that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

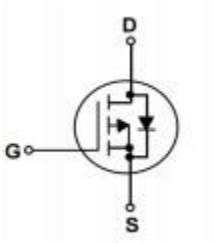
GENERAL FEATURES

- V_{DS}=-30V, I_D=-50A
  $R_{DS(ON)}$(Typ.)=5.8mΩ @ V_{GS}=-10V
  $R_{DS(ON)}$(Typ.)=8mΩ @ V_{GS}=-4.5V
- Advanced High Cell Density Trench Technology
- Low Gate Charge
- 100% EAS Guaranteed
- Green Device Available

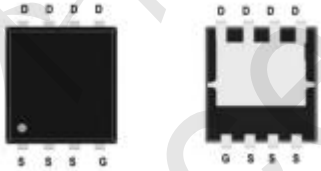
APPLICATION

- Power Management Switches
- Battery Protection Application

PINOUT



Schematic diagram



DNF3x3 top and bottom view

ORDERING INFORMATION

Part Number	StorageTemperature	Package	Devices Per Reel
MXN3349	-55°C to 150°C	DFN3x3	5000

ABSOLUTE MAXIMUM RATINGS(T_A=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous(T_C=25°C)	I_D	-50	A
Drain Current-Continuous(T_C=100°C)	I_D	-32	A
Pulsed Drain Current(Note1)	I_{DM}	-200	A
Single Pulse Avalanche Energy(Note2)	E_{AS}	80	mJ
Total Power Dissipation(T_C=25°C)	P_D	69	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	°C
Thermal Resistance, Junction-to-Ambient(Note3)	$R_{\theta JA}$	65	°C/W
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.8	°C/W

Note 1. Pulse width limited by maximm junction temperature $T_{J(MAX)}$=150°C

Note 2. The EAS data shows Max. rating. The test condition is V_{DD}=-25V, V_{GS}=-10V, L=0.1mH, I_{AS}=-40A.

Note 3. The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.

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ELECTRICAL CHARACTERISTICS(T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=-250μA	-30	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-30V, V_{GS}=0V	-	-	-1	μA
		V_{DS}=-30V,V_{GS}=0V,T_J=100°C	-	-	-100	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=-250μA	-1.0	-	-2.5	V
Drain-Source On-State Resistance(Note1)	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-20A	-	5.8	8	mΩ
		V_{GS}=-4.5V, I_D=-15A	-	8	13.5	mΩ
Forward Transconductance(Note1)	g_{FS}	V_{DS}=-10V, I_D=-20A	-	50	-	S
Dynamic Characteristics(Note2)						
Input Capacitance	C_{iss}	V_{DS}=-15V, V_{GS}=0V, F=1.0MHz	-	3512	-	pF
Output Capacitance	C_{oss}		-	463	-	pF
Reverse Transfer Capacitance	C_{rss}		-	369	-	pF
Gate Resistance	R_g	F=1.0MHz	-	9.3	-	Ω
Switching Characteristics(Note2)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=-15V, I_D=-20A, V_{GS}=-10V, R_G=3Ω	-	10.8	-	nS
Turn-on Rise Time	t_r		-	13.2	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	73	-	nS
Turn-Off Fall Time	t_f		-	35	-	nS
Total Gate Charge	Q_g	V_{DS}=-15V, I_D=-20A, V_{GS}=-10V	-	34	-	nC
Gate-Source Charge	Q_{gs}		-	9.9	-	nC
Gate-Drain Charge	Q_{gd}		-	10.4	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage(Note1)	V_{SD}	V_{GS}=0V, I_S=-1A	-	-	-1.2	V
Continuous Source Current(T_C=25°C)	I_{SD}	-	-	-	-50	A
Reverse Recovery Time	t_{rr}	I_F=-20A, dI/dt=100A/μS	-	25	-	nS
Reverse Recovery Charge	Q_{rr}		-	10	-	nC

Note 1. The data tested by pulsed, pulse width ≤ 300us , duty cycle ≤ 2%.
Note 2. This value is guaranteed by design hence it is not included in the production test.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

Figure 1. Output Characteristics

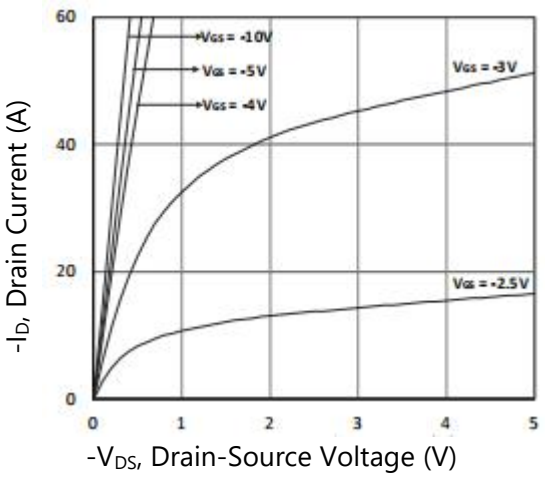


Figure 2. Transfer Characteristics

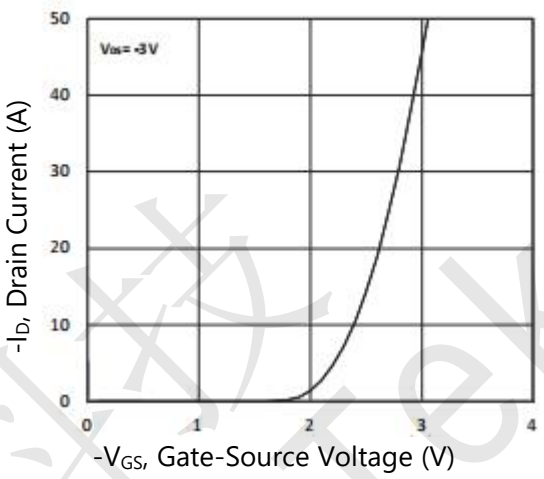


Figure 3. Normalized $R_{DS(ON)}$ vs Temperature

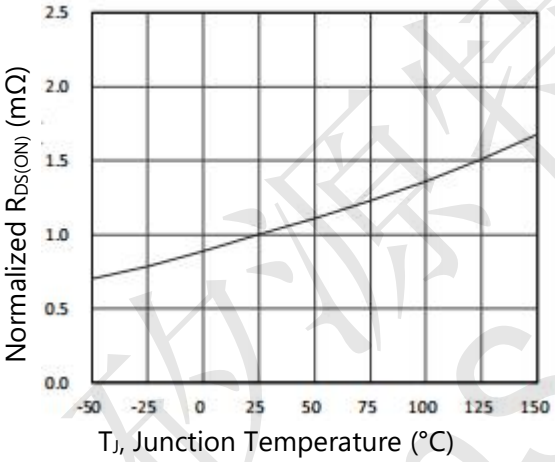


Figure 4. $R_{DS(ON)}$ vs V_{GS}

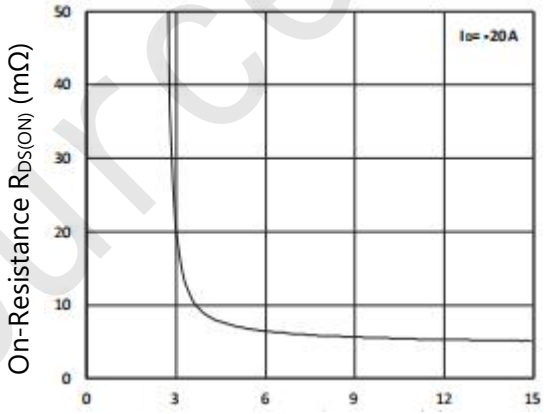


Figure 5. $R_{DS(ON)}$ vs I_D

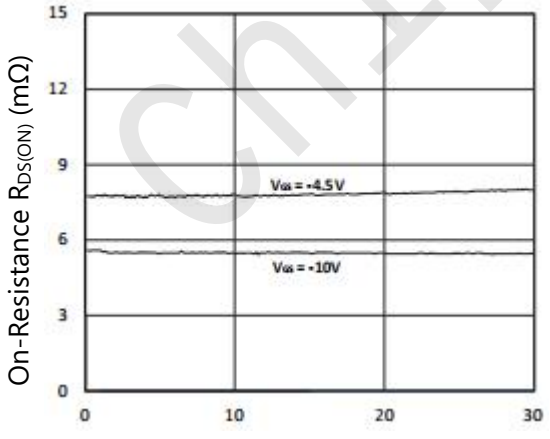
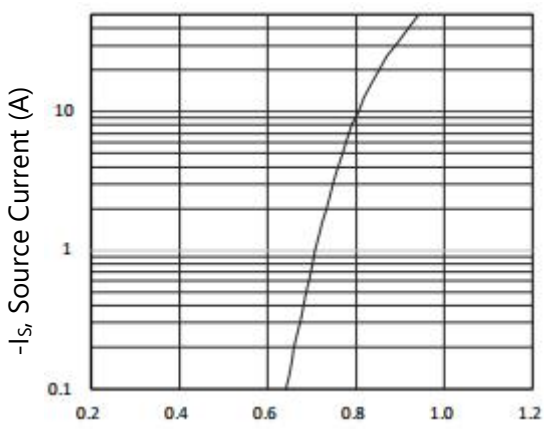


Figure 6. Forward Characteristics of Reverse



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

Figure 7. Capacitance Characteristics

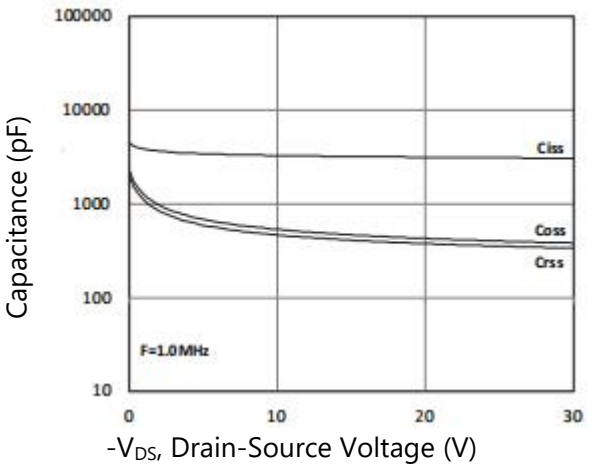


Figure 8. Safe Operating Area

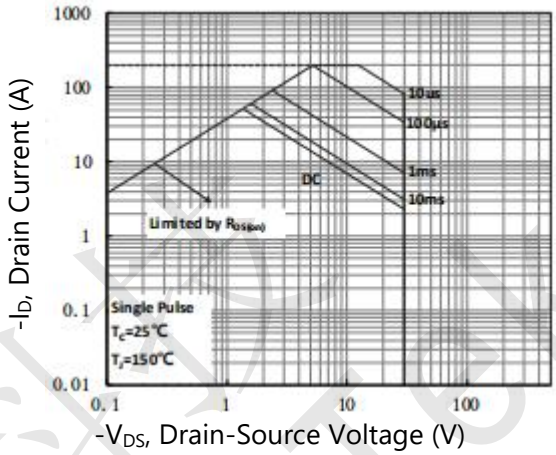


Figure 9. Transfer Characteristics

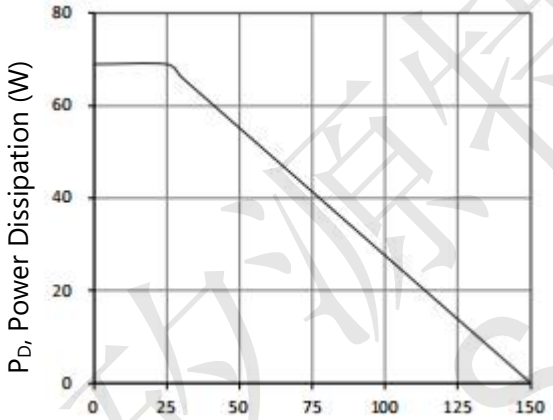


Figure 10. Normalized Threshold Voltage

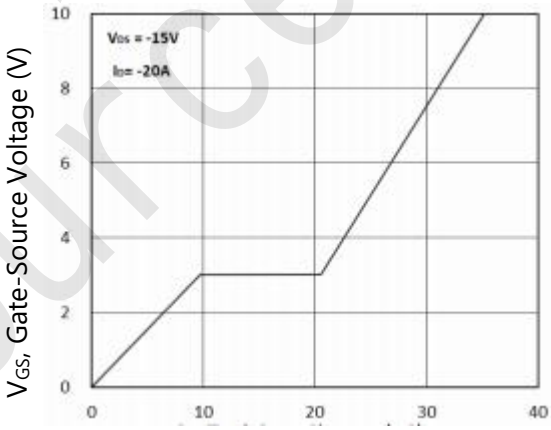
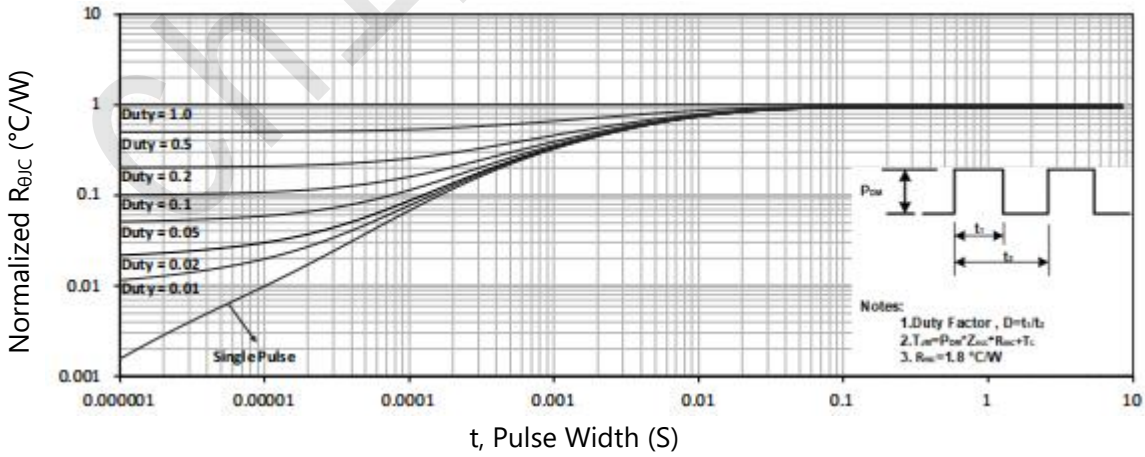


Figure 11. Normalized Maximum Transient Thermal Impedance



TEST CIRCUIT

Figure 1. Gate Charge Test Circuit & Waveforms

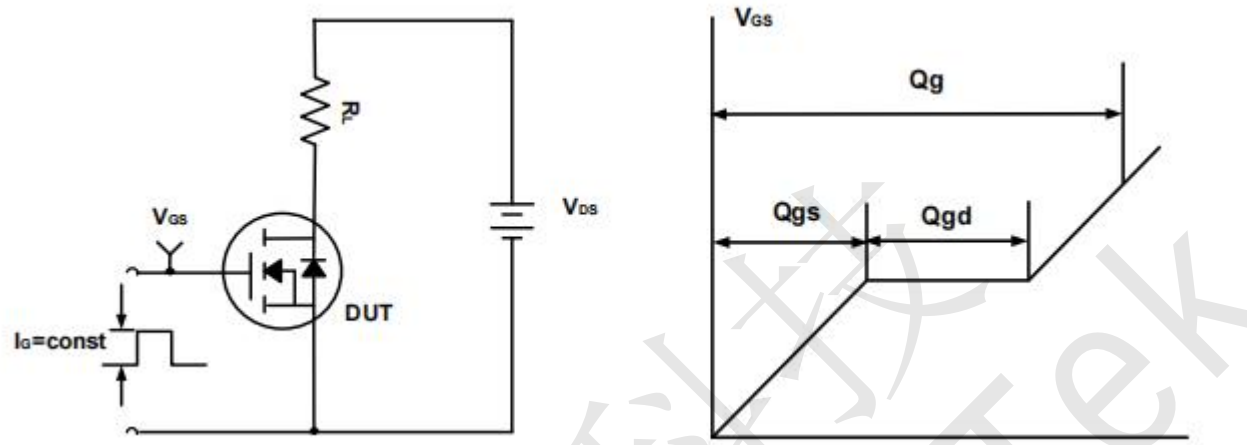


Figure 2. Switching Test Circuit & Waveforms

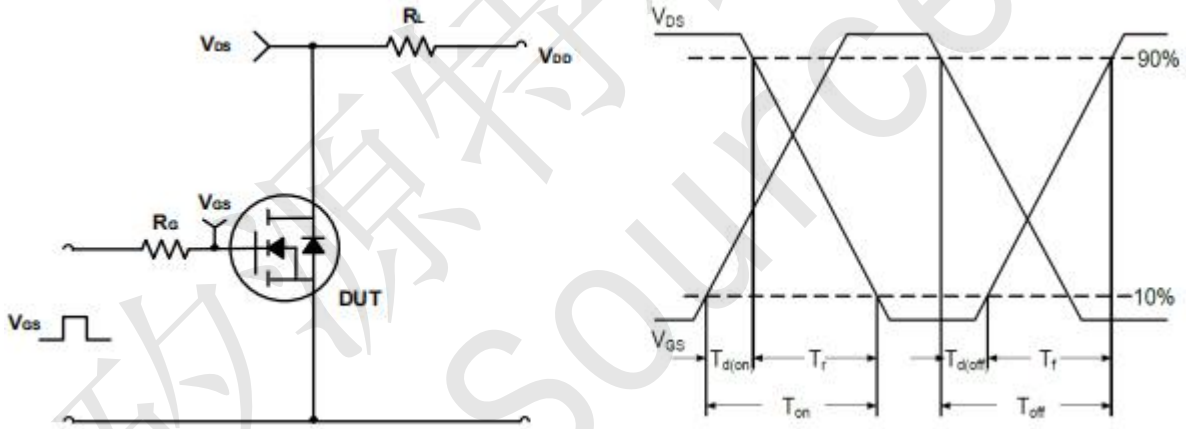
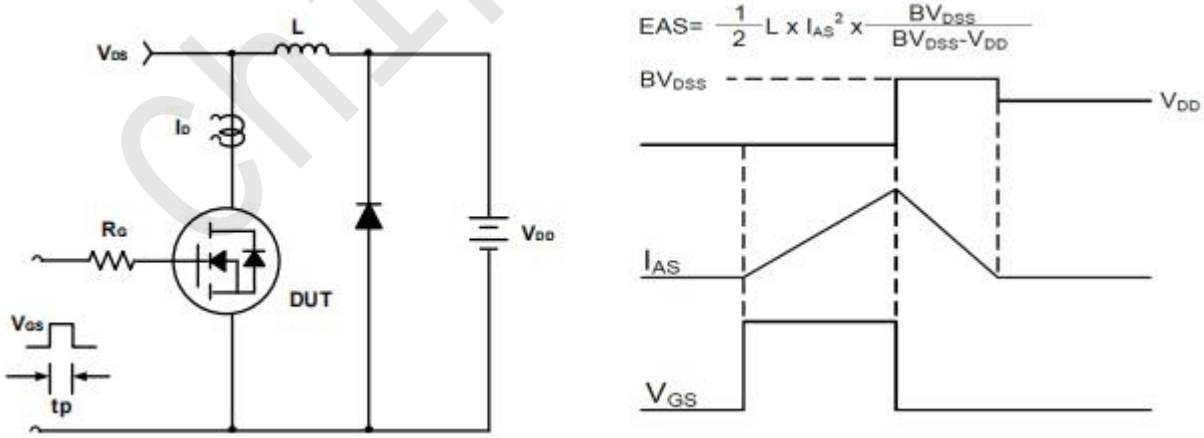
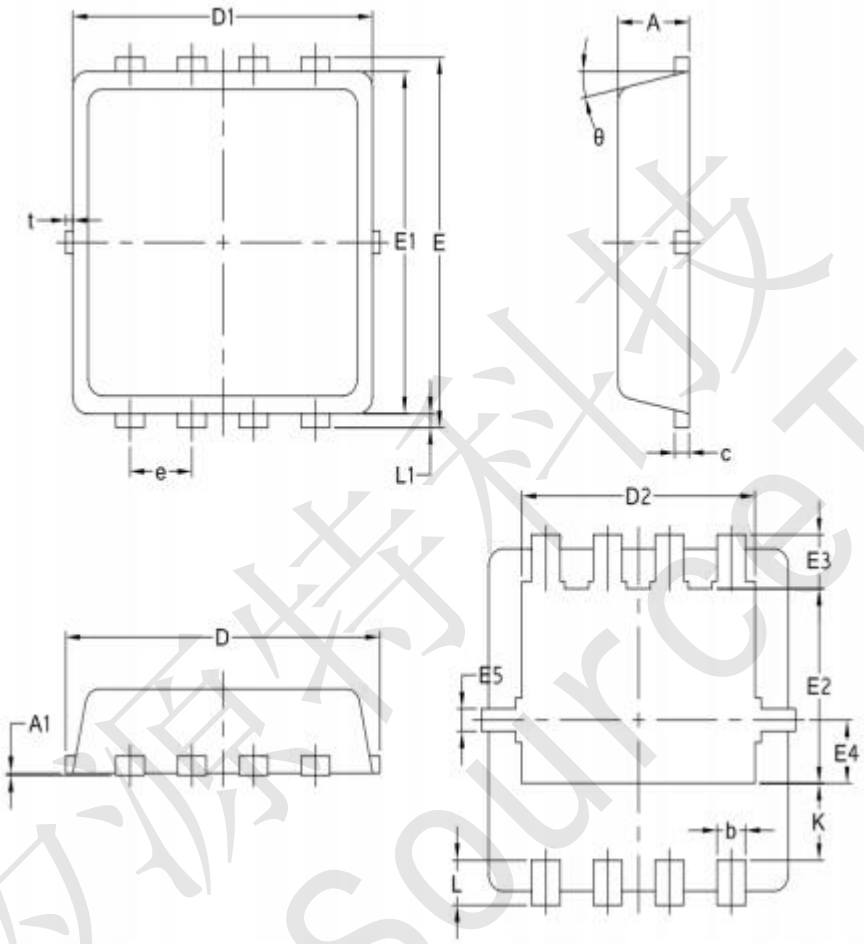


Figure 3. Unclamped Inductive Switching Circuit & Waveforms



PACKAGE INFORMATION

DFN3x3-8L



Symbol	Dimensions In Millimeters			Symbol	Dimensions In Millimeters		
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.
A	0.70	0.75	0.85	E3	0.28	0.48	0.65
A1	-	-	0.05	E4	0.37	0.57	0.77
b	0.20	0.30	0.40	E5	0.10	0.20	0.30
c	0.10	0.152	0.25	e	0.60	0.65	0.70
D	3.15	3.30	3.45	K	0.59	0.69	0.89
D1	3.00	3.15	3.25	L	0.30	0.40	0.50
D2	2.29	2.45	2.65	L1	0.06	0.125	0.20
E	3.15	3.30	3.45	t	0	0.075	0.13
E1	2.90	3.05	3.20	θ	10°	12°	14°
E2	1.54	1.74	1.94				