CST5182A/5171A/5171S1/5086A Speech IC

1. CST5182A/5171A/5171S1/5086A General Descriptions

CST5182A/5171A/5171S1/5086A series are 4-bits micro-controller which could play 4 channel melody or 4 channels ADPCM with PWM direct drive circuit. The CST series are OTP (One Time Programmable) type memory, and CSTM series are MASK type memory. PWM resolution is 8/10/12 bits. They included a low cost, high performance CMOS micro-processor. The clock frequency of this up is typically 8.192 (±3%) MHz. This chip operates over a wide voltage range of 2.0V~5.5V. It contains program ROM (PROM) and data ROM (DROM) inside. The maximum program ROM (PROM) is 16K words and maximum data ROM (DROM) size is 544K byte. The maximum working SRAM is (256+2) nibbles. It is provided with total 16 software programmable I/O ports and 4 outputs (defined by options).

2. CST5182A/5171A/5171S1/5086A Features

- Operating voltage: **2.0V to 5.5V**
- MCU Operation frequency: **8.192MHz**
- Memory Size
  - Program ROM size: **Maximum 16K*12 bits OTP type**
  - Data ROM size: **Maximum 544K*8 bits OTP type**
  - SRAM size: **256*4 bits**
  - User register: **2*4 bits**
- Wakeup function for power-down mode:
  - HALT mode wakeup source: Port A, Port B, Port D and Port E can wake-up from HALT mode to NORMAL mode and executing wake-up sub-routine program.
- 12 input/output pins: Port A, Port B and Port D can be defined as input or output port bit by bit.
- 4 output pins: Port C.
- 4 input/output or 4 input pins defined by option: If input pins are employed, Port E is defined as input ports. If input/output pins are selected, Port E is defined as input or output port bit by bit.
- Four reset condition:
  - Low voltage reset.
  - Power on reset.
  - External reset pin. (active low)
  - Watch dog timer overflow.
- One internal interrupt sources:
  - PWM interrupt.
- WDT
  - Watch dog timer, can enabled/disabled by option.
  - WDT period is 256*256*16/Fsys. (WDT period is 0.13 sec for system clock=8.192MHz)
- Audio output:
  - Support PWM or DAC mode by option. **(Only CST series are provided DAC function)**
  - Support 8/10/12 bits.
- Support option set for pull down resistor 1M, 50K or 220K Ohm, reset pin (PB3 or PC3), low voltage reset…etc.
- Oscillator fuse option ±3%, temperature & voltage compensation.
- Support security option (1 bit) for read inhibition.

CST5182A/5171A/5171S1/5086A Speech IC

The I/O ports, RAM, ROM sizes and functions table of CST5182A/5171A/5171S1/5086A are shown below：

Body	CST5182A	CST5182A	CST5171A	CST5171A	CST5171S1	CST5086A	CST5086A
Voice duration	182 sec.		170 sec.			85 sec.	
RAM size	(256+2)*4-bits		(256+2)*4-bits			(256+2)*4-bits	
I/O pins	12 I/O + 4O + 4I 16 I/O + 4O		12 I/O + 4O + 4I 16 I/O + 4O		16 I/O	12 I/O + 4O + 4I 16 I/O + 4O	
PROM size	16K*12-bits		16K*12-bits			16K*12-bits	
DROM size	544K*8-bits		512K*8-bits			256K*8-bits	
DAC	X	O	X	O	X	X	O
OP amp	X	O	X	O	X	X	O
Comparator	X	O	X	O	X	X	O

3. CST5182A/5171A/5171S1/5086A Packaging and Pads Information

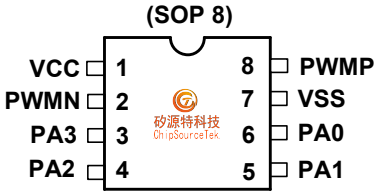
3.1 Pads

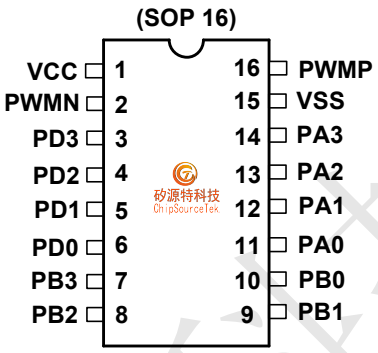
PAD Name	Type	State After Reset	Description
Reset, Power Input			
VDD	P	High	Power input of I/O port.
VSS	P	Low	Ground input except PWM block power. It could be double bonded with VPS pad.
VPD	P	High	PWM block power input in normal operation.
VPS	P	Low	The ground pad of PWM block. It could be double bonded with VSS pad.
General I/O ports			
PA3~PA0	I/O	XXXX	Port A is a programmable Input /Output port.
PB3~PB0	I/O	XXXX	Port B is a programmable Input /Output port. PB3 can be employed as reset pin according to the option.
PC3~PC0	O	XXXX	Port C is an output port only. PC3 can be employed as reset pin according to the option.
PD3~PD0	I/O	XXXX	Port D is a programmable Input /Output port.
PE3~PE0	I or I/O	XXXX	Port E is an Input port or programmable Input/Output port defined by option.
Audio output pads			
PWMP	O	Low	Audio output PWM(+).
PWMN	O	Low	Audio output PWM(-).

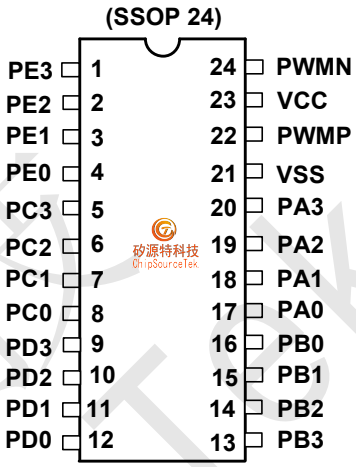
Table 1: Pad Description

3.2 Package

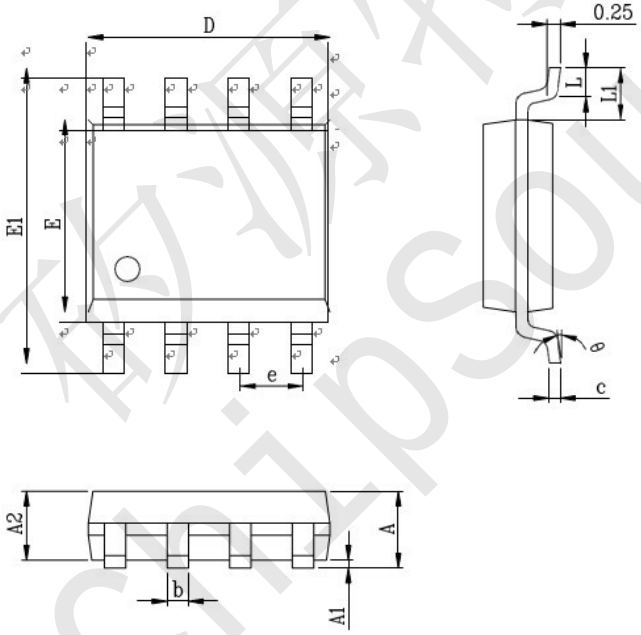
CST5182A/5171A/5086A provides SOP8, SOP16, SSOP24







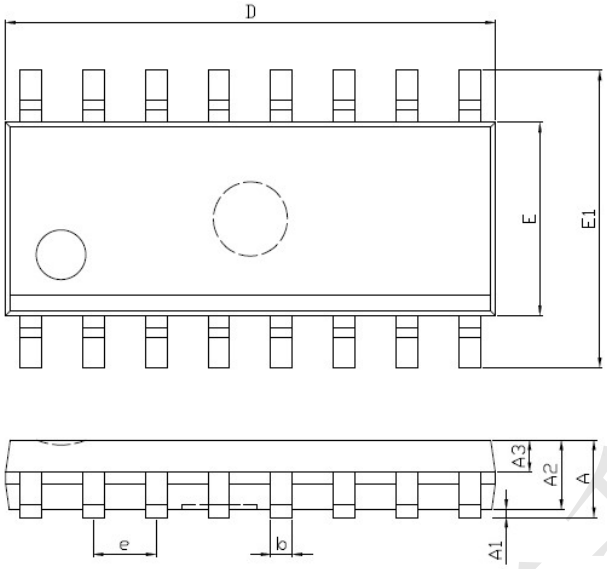
3.2.1 SOP8

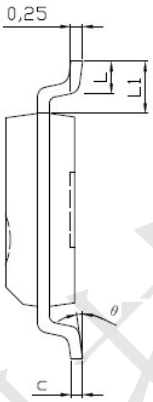


Symbol	Dimensions In Millimeters	
	Min	Max
A	1.35	1.75
* A1	0.10	0.23
A2	1.30	1.50
* b	0.39	0.45
c	0.21	0.26
D	4.70	5.10
E	3.70	4.10
* E1	5.80	6.20
* e	1.24	1.30
* L	0.50	0.80
* L1	0.99	1.10
θ	0°	8°

注:1.標注"*"尺寸爲測量尺寸

3.2.2 SOP16

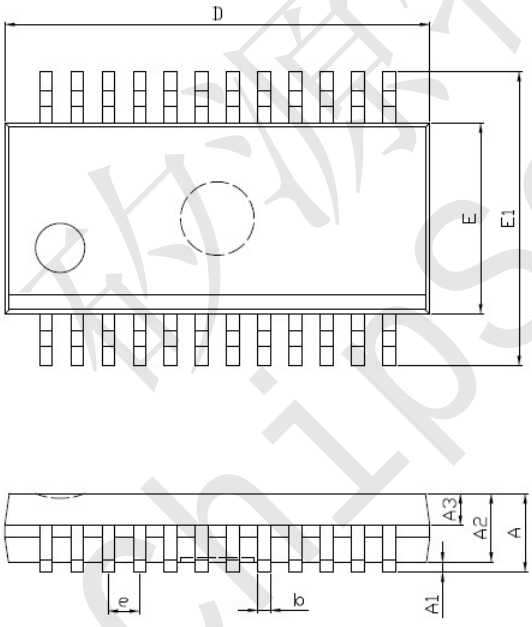


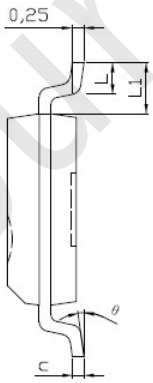


Symbol	Dimensions In Millimeters	
	Min	Max
A		1.75
* A1	0.10	0.25
A2	1.40	1.50
A3	0.61	0.71
* b	0.39	0.45
c	0.21	0.26
D	9.70	10.10
E	3.70	4.10
* E1	5.80	6.20
* e	1.24	1.30
* L	0.60	0.80
* L1	0.99	1.10
θ	0°	8°

注1.标注“*”尺寸为测量尺寸。

3.2.3 SSOP24





Symbol	Dimensions In Millimeters	
	Min	Max
A	1.35	1.75
* A1	0.10	0.25
A2	1.40	1.50
* b	0.23	0.30
c	0.21	0.26
D	8.45	8.85
E	3.70	4.10
* E1	5.80	6.20
* e	0.61	0.66
* L	0.50	0.80
* L1	0.99	1.10
θ	0°	8°

注1.标注“*”尺寸为测量尺寸。

3.3 Block Diagram

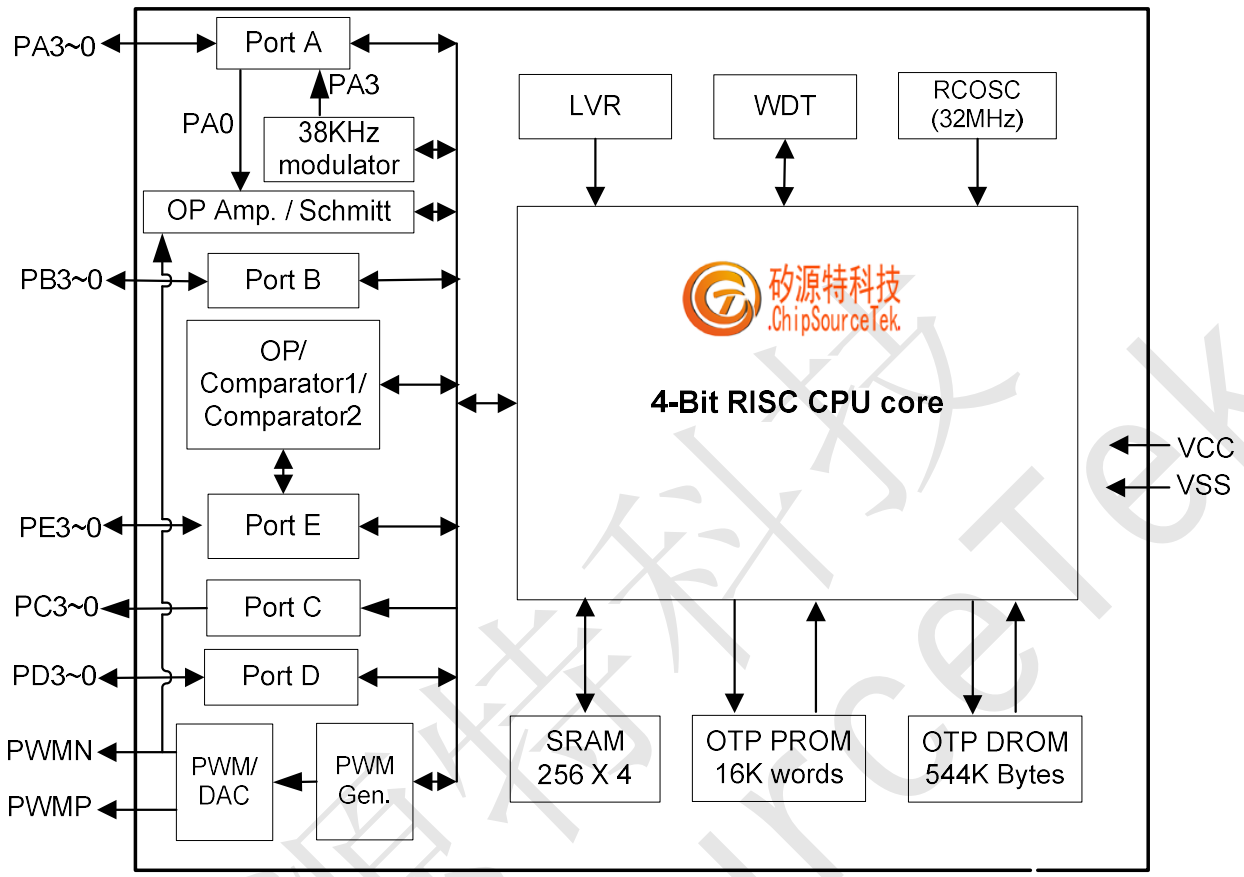


Figure1. Block diagram

4. CST5182A/5171A/5171S1/5086A ELECTRICAL CHARACTERISTICS

4.1 Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
DC Supply Voltage	Vcc	-0.5 to 6.0	V
Input Voltage	Vin	-0.5 to Vcc+0.5	V
Operating Temperature Range	Ta	0 to +75	℃
Storage Temperature Range	Tstg	-25 to +85	℃

Table 2: Absolute Maximum Ratings

4.2 DC Characteristics

VCC=3.0V, Ta=25℃ unless otherwise noted.

Parameters	Symbol	Minimum	Typical	Maximum	Condition
Power supply range	Vcc	2.0 V	-	5.5 V	
OTP Programming Power	Vpp	9.5 V	10 V	10.5 V	V_{CC} = 4.8V
Supply current	Iop		5mA		System clock 8.192MHz PWM disabled
Stand-by Current (RCWK disabled)	I_{STBY_A}		3uA		VCC=5.0V, MCU halt PA0 RCWK option disabled
Standby Current (RCWK enabled)	I_{STBY_B}		8uA		VCC=5.0V, MCU halt PA0 RCWK option enabled (Wake-up 4 times per second)
Input high voltage	Vih	0.8 VCC			
Input low voltage	Vil			0.2 VCC	
Input leakage current	Ilk		0.1 uA		
Output high voltage	Voh	0.95 VCC			no load
Output low voltage	Vol			0.05 V	no load
Output high current in high source capacity mode	Ioh0		20mA		Vout=2.0 all ports High source capacity
Output low current in high sink capacity mode	Iol0		-20mA		Vout=1.0 all ports High sink capacity
Output high current in normal source capacity mode	Ioh1		4mA		Vout=2.0 all ports Normal source capacity
PWM output load		-		8 ohm	Speaker impedance
Pull up resistor of PB3, PC3	Rrst	-	30K Ohm	-	Pins with pull up of PB3 or PC3 reset pins
Pull-down resistance	Rpd1	-	50K Ohm	-	Pins with pull-down of PA, PB, PD and PE
Pull-down resistance	Rpd2		220K Ohm		Pins with pull-down of PA, PB, PD and PE
Pull-down resistance	Rpd3		1M Ohm		Pins with pull-down of PA, PB, PD and PE

Table 3: DC Characteristics

4.3 AC Characteristics

VCC=3.0V, Ta=25℃ unless otherwise noted.

Parameters	Symbol	Minimum	Typical	Maximum
Operating Frequency(RC Oscillator)	Fsys	7.946MHz	8.192 MHz	8.43MHz
RC reset time-constant	Trrc	-	10 us	-
Data ROM data ready time	Tdrr	-	-	2/Fsys
Wake-up time-constant	Twk		250us	

Table 4: AC Characteristics

5. CST5182A/5171A/5171S1/5086A FUNCTIONAL DESCRIPTION

This chapter describes the function of MCU.

5.1 Program ROM (PROM)

The PROM is an OTP (One Time Programmable) type memory. The maximum size of **PROM is 16K*12-bits (0000H ~ 3FFFH)** which stores execution program. The last 256 location of effective PROM is reserved area for testing program. The user shall not use this area in any case. Assembler shall check user program on this limit. Hardware does not need to check this restriction.

In order to reserve unused area of PROM. These regions maybe use in the future. There is one option "OTPREV" for this purpose. If all unused area of PROM want to fill with "0XFFF", the option "OTPREV" on IDE tool must be enabled. Otherwise, they will fill with "0x000".

PROM address	Function description
0x0000 ~ 0x0001	Reset
0x0004 ~ 0x0005	Wake-up
0x0008 ~ 0x0009	Interrupt
0x000A ~ 0x3EFF	User code
0x3F00 ~ 0x3FFF	Reserve area

Table 5: Memory Map of PROM

5.2 Data ROM (DROM)

The DROM is an OTP (One Time Programmable) type memory. The maximum size of **DROM is 544K*8-bits** which stores the 8-bits wide data for ADPCM or melody data …etc. The last 64 location is a reserved area. The user shall not use this area in any case. Assembler shall check user data ROM on this limit. Hardware does not need to check this restriction.

DROM address (DMA)	Function description
0x00000 ~ 0x000FF	User area
0x00100 ~ 0x001FF	User area
0x00200 ~ 0x002FF	User area
…	…
0x3FB00 ~ 0x3FBBF	User area (Max. size of CST(M)5086A)
…	…
0x7FF00 ~ 0x7FFBF	User area (Max. size of CST(M)5171A / CST5171S1)
…	…
0x87F00 ~ 0x87FBF	User area (Max. size of CST(M)5182A)
0x87FC0 ~ 0x87FFF	System area, last 64 location(don't use it)

Table 6: Memory Map of DROM

DROM is addressed by five registers DMA4, DMA3, DMA2, DMA1 and DMA0. After these registers are specified by software, the data need enough delay time, Tdrr in the table of "AC Characteristics". After this delay time, the data can be read from data register (DMDL & DMDH). Otherwise, the data you read will be unknown. Read DROM Data must enter "NOP" after command "LD", "CMP", "SUB", "ADC", "AND", "OR" or "XOR" both "DMDL" and "DMDH".

Ex:

```
LD      (DMA0), A
…
LD      (DMA4), A       ; Set DMA0~4
LD      A, (DMDL)       ; Read low nibble data from DROM, address as DMA4~0.
NOP                     ; Must be “NOP”
LD      A, (DMDH)       ; Read high nibble data from DROM, address as DMA4~0.
NOP                     ; Must be “NOP”
```

Symbol	Addr	R/W type	Reset	D3	D2	D1	D0	Description
DMA0	18H	R/W	xxxx	DMA0.3	DMA0.2	DMA0.1	DMA0.0	DMA0~4, five register built a 18-bits addressing space for read DROM 8-bits data. DMA0 is lowest nibble, DMA4 is highest nibble of DROM address.
DMA1	19H	R/W	xxxx	DMA1.3	DMA1.2	DMA1.1	DMA1.0	
DMA2	1AH	R/W	xxxx	DMA2.3	DMA2.2	DMA2.1	DMA2.0	
DMA3	1BH	R/W	xxxx	DMA3.3	DMA3.2	DMA3.1	DMA3.0	
DMDL	1CH	R/W	xxxx	DMDL.3	DMDL.2	DMDL.1	DMDL.0	Low nibble of DROM data read from this address.
DMDH	1DH	R/W	xxxx	DMDH.3	DMDH.2	DMDH.1	DMDH.0	High nibble of DROM data read from this address. Write this register means reset watch dog timer if this timer is enabled by option.
DMA4	1EH	R/W	xxxx	DMA4.3	DMA4.2	DMA4.1	DMA4.0	DMA4 is highest nibble of DROM address

Table 7: SFRs about DROM

5.3 SRAM and Special Function Register

5.3.1 SRAM

There are **256 nibbles SRAM** in this chip. The SRAM and I/O memory map is divided into several pages by setting MAH register (3 bits wide). The initial value of MAH is unknown and must be defined by instructions “LDMAH” before you utilize SRAM. The extra 2 SRAM nibbles in the specifications and hardware manuals of relative mask ROM products are not SRAM in fact. They are USER1 and USER2 of SFRs.

Direct Addressing		SRAM MAP
MAH=XH	00H~1FH	SFR(special function register) register
MAH=0H	20H~3FH	USER SRAM
MAH=1H	20H~3FH	
~	20H~3FH	
MAH=7H	20H~3FH	

Table 8: Memory Map of SFRs

The first 32-nibble, 00H ~ 1FH, are defined as a common block. Some I/O and user register is arranged in this common block for easy data operations. The other regions, 20H~3FH, are employed as SRAM.
The user must notice that the initial content of SRAM is unknown.

5.3.2 Special Function Registers

The special function register consists of common I/O and other special register.
A special function register supports LD/ADC/SBC/OR/AND/XOR/INC/DEC/RLC/RRC/CMP/ADR operation. Bit set/clear can only be operated on the address range from 00H to 0FH, except indirect operation is used.
The following table describes all of the SFRs.

Symbol	Addr	R/W type	Reset	D3	D2	D1	D0	Description
STATUS	00H	R/W	00xx	reserved	PWFG	CF	ZF	Status Register PWFG: PWM interrupt flag. CF: Carry flag. ZF: Zero flag.
IOC_PE	01H	R/W	0000	IOCE3	IOCE2	IOCE1	IOCE0	Enable when option “PEIO” selected. “1” = output, “0” = input of related PE bit.
IOC_PA	02H	R/W	0000	IOCA3	IOCA2	IOCA1	IOCA0	“1” = output, “0” = input of related PA bit.
DATA_PA	03H	R/W	xxxx	DPA3	DPA2	DPA1	DPA0	Read from Port A input port and write to output port.
DATA_PC	04H	R/W	0000	DPC3	DPC2	DPC1	DPC0	Port C is output port only. Write to Port C output port.
IOC_PB	05H	R/W	0000	IOCB3	IOCB2	IOCB1	IOCB0	“1” = output, “0” = input of related PB bit.
DATA_PB	06H	R/W	xxxx	DPB3	DPB2	DPB1	DPB0	Read from Port B input port and write to output port.
USER1	07H	R/W	xxxx	USER1.3	USER1.2	USER1.1	USER1.0	General purpose user register.
AUD_DL	08H	W	xxxx	AUD_DL3	AUD_DL2	AUD_DL1	AUD_DL0	AUD_DL[3:2]: The bit1~0 of 10-bits PWM, combine with AUD_DM[3:0], AUD_DH[3:0] to built 10-bits PWM if option PWM10 is 1 and PWM12 is 0. AUD_DL[3:0]: The bit3~0 of 12-bits PWM, combine with AUD_DM[3:0], AUD_DH[3:0] to built 12-bits PWM if option PWM12 is 1.
SYS0	09H	R/W	--x0	reserved	reserved	ENINT	ENPWM	ENPWM: “1” Enable PWM, “0” Disable PWM. ENINT: Enable global interrupt.
AUD_DM	0AH	W	xxxx	AUD_DM3	AUD_DM2	AUD_DM1	AUD_DM0	AUD_DM[3:0]: The low nibble of 8-bits PWM. The bit5~2 of 10-bits PWM. The bit7~4 of 12-bits PWM.
AUD_DH	0BH	W	xxxx	AUD_DH3	AUD_DH2	AUD_DH1	AUD_DH0	AUD_DH[3:0]: The high nibble of 8 bits PWM. The bit9~6 of 10 bits PWM. The bit11~8 of 12 bits PWM. Note: AUD_DH3 is sign bit, “0” means positive.
IOC_PD	0CH	R/W	0000	IOCD3	IOCD2	IOCD1	IOCD0	“1” = output, “0” = input of related PD bit.
DATA_PD	0DH	R/W	xxxx	DPD3	DPD2	DPD1	DPD0	Read from Port D input port and write to output port.
DATA_PE	0EH	R/W	xxxx	DPE3	DPE2	DPE1	DPE0	Port E defined as I/O port or input port depends on option PEIO. Read from Port E input port and write to output port.
USER2	0FH	R/W	xxxx	USER2.3	USER2.2	USER2.1	USER2.0	General purpose user register.
IADJ	10H	R/W	xx00	-	-	ADJ1	ADJ0	ADJ[1:0]: Adjust the frequency, when enable option OPTADJ. ADJ[1:0] / Frequency % 00 / -4% 01 / -2% 10 / 2% 11 / 4%
Reserved	11H~17H	-	xxxx	-	-	-	-	Reserved
DMA0	18H	R/W	xxxx	DMA0.3	DMA0.2	DMA0.1	DMA0.0	DMA0~4, five register built a 19-bits addressing space for read DROM 8-bits
DMA1	19H	R/W	xxxx	DMA1.3	DMA1.2	DMA1.1	DMA1.0	

DMA2	1AH	R/W	xxxx	DMA2.3	DMA2.2	DMA2.1	DMA2.0	data, DMA0 is lowest nibble, DMA4 is highest nibble of DROM address.
DMA3	1BH	R/W	xxxx	DMA3.3	DMA3.2	DMA3.1	DMA3.0	
DMDL	1CH	R/W	xxxx	DMDL.3	DMDL.2	DMDL.1	DMDL.0	Low nibble of DROM data read from this address.
DMDH	1DH	R/W	xxxx	DMDH.3	DMDH.2	DMDH.1	DMDH.0	High nibble of DROM data read from this address. Writing this register means reset watch dog timer if this timer is enabled by option.
DMA4	1EH	R/W	xxxx	DMA4.3	DMA4.2	DMA4.1	DMA4.0	DMA4 is highest nibble of DROM address.
Reserved	1FH	-	xxxx	-	-	-	-	Reserved

Table 9: All of the Special Function Registers

5.4 Interrupt Vector Address

Vector	Address
RESET	00H
WAKEUP	04H
INT	08H

Table 10: Interrupt Vectors

5.5 Interrupt Controller

There is only one interrupt entry point in this chip. Normally interrupt period is 32768Hz. It can be changed to 65536Hz by option “PWM64K”. Program will jump to address $008h when an interrupt occurs.

Symbol	Addr	R/W type	Reset	D3	D2	D1	D0	Description
STATUS	00H	R/W	00xx	reserved	**PWFG**	CF	ZF	Status Register **PWFG: PWM interrupt flag.** CF: Carry flag. ZF: Zero flag.
SYS0	09H	R/W	--x0	reserved	reserved	**ENINT**	**ENPWM**	**ENPWM: “1” Enable PWM, “0” Disable PWM.** **ENINT: Enable global interrupt.**

Table 11: SFRs about Interrupt

If the global interrupt enable bit (INTEN) is high and interrupt request (PWFG=1) occurred, then interrupt will be accepted on next clock. On that instant, current (next) program counter, PCDH, MAH and C/Z will be stored in special hardware registers, and program counter will be loaded with entry address of that interrupt. All these are done in one clock. Interrupt enable bit will be cleared too. As long as program enters interrupt service, interrupt enable bit is cleared. It's no need to clear interrupt enable flag in interrupt routine. But hardware will not clear interrupt request flag (PWFG). Software is required to clear it.

When interrupt service routine is done, an RETI shall be executed. This instruction will restore stored program counter, PCDH, MAH and C/Z, will set interrupt enable bit=1 also. (Note that RETI is different from RETS.) Interrupt request can be accepted only when enable bit be set. Note that only one level of INT routine can be used.

5.6 Clock Operation

There are two operation modes in this chip. The state diagram of MCU operation modes is shown below:

1. NORMAL Mode: In normal mode, system clock oscillator is running, and MCU clock source is come from main oscillator. In NORMAL mode, MCU will go to halt mode after HALT instruction executed.

2. HALT Mode: In HALT mode, the MCU clock stops, users can't change the operation mode when in halt mode. It will go back to NORMAL mode (Program counter=$004) when I/O wakeup or reset occurred. Please refer to the section of" Halt Mode & Wake up" for the detailed HALT mode description.

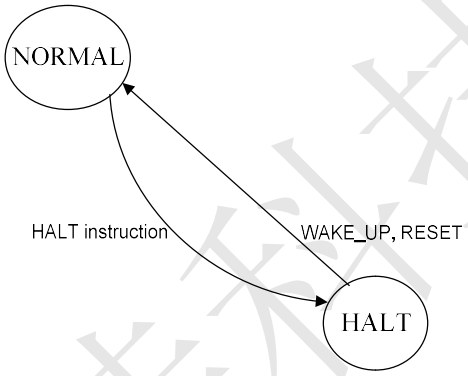


Figure 2: Clock Operation Mode

5.7 Halt Mode & Wake up

The MCU is changed into HALT mode (program counter and system clock stop) when HALT instruction executed. It provides a power saving mode for those applications requiring a very low stand-by current. The PA[3:0], PB[3:0], PD[3:0] and PE[3:0] are supporting the wake-up function when rising edge occurred.

The program counter will be $004H when HALT instruction executed immediately, then program counter will go to next address after 64 stable clock(system clock) when wake up condition occurred. Reset signal will release HALT state and execute reset procedure because reset is first priority when in HALT mode, so program counter will from $004h to $000h, program counter goes to next address after 64 stable clock cycles. Furthermore, the SRAM will keep their previous data without changing in this mode.

5.8 Watch Dog Timer Reset (WDT)

The watch dog timer (WDT) is used to reset whole chip when detect unexpected execution sequence caused by accident condition, avoiding dead lock of MCU program. WDT will be reset when wake-up from halt, after reset or software clears it. The watch dog timer is a simple counter. It has a fixed length of 256*256*16/system-clock (ex: 0.13 sec for 8.192MHz system clock) after the clearance of watch dog.

Software must run a "clear watch dog timer" (write to DMDH) instruction before this timer time out when WDT enabled. It will generate a reset signal to reset whole system when WDT over flow. Assembler will check user program about the "reset watch dog" instructions. If more than one "reset watch dog" is found in program, assembler will generate a warning (program code will still be generated). "HALT" instruction will reset watch dog timer. The reset watch dog timer sequence is strongly recommended as:

```
WATCHDOG:
        LD      (1DH), A
```

5.9 8/10/12 Bits PWM/DAC

There are three optional PWM/DAC output resolutions. One is 8-bits output, the sec. is 10-bits output, and the other is 12-bits output. The highest of input data is signed bit: '0' represents positive, '1' represents negative.

CSTM series only supports audio output with PWM mode. CST series supports audio output with PWM and DAC two modes. These two modes can be selected by "DACEN" option. If use DAC output mode, option "DACEN" must be enabled. Otherwise, PWM mode is enabled. All PWM registers will be exchanged for DAC mode if "DACEN" option is enabled.

Symbol	Addr	R/W type	Reset	D3	D2	D1	D0	Description
STATUS	00H	R/W	00xx	reserved	**PWFG**	CF	ZF	Status Register **PWFG: PWM interrupt flag.** CF: Carry flag. ZF: Zero flag.
AUD_DL	08H	W	xxxx	**AUD_DL3**	**AUD_DL2**	**AUD_DL1**	**AUD_DL0**	**AUD_DL[3:2]:** The bit1~0 of 10-bits PWM, combine with AUD_DM[3:0], AUD_DH[3:0] to built 10-bits PWM if option PWM10 is 1 and PWM12 is 0. **AUD_DL[3:0]:** The bit3~0 of 12-bits PWM, combine with AUD_DM[3:0], AUD_DH[3:0] to built 12-bits PWM if option PWM12 is 1.
SYS0	09H	R/W	--x0	reserved	reserved	**ENINT**	**ENPWM**	**ENPWM: "1" Enable PWM, "0" Disable PWM.** **ENINT: Enable global interrupt.**
AUD_DM	0AH	W	xxxx	**AUD_DM3**	**AUD_DM2**	**AUD_DM1**	**AUD_DM0**	**AUD_DM[3:0]:** The low nibble of 8-bits PWM. The bit5~2 of 10-bits PWM. The bit7~4 of 12-bits PWM.
AUD_DH	0BH	W	xxxx	**AUD_DH3**	**AUD_DH2**	**AUD_DH1**	**AUD_DH0**	**AUD_DH[3:0]:** The high nibble of 8 bits PWM. The bit9~6 of 10 bits PWM. The bit11~8 of 12 bits PWM. Note: AUD_DH3 is sign bit, "0" means positive.

Table 12: SFRs about the operation of PWM

5.9.1 8-Bits PWM/DAC

This PWM is 8-bits output resolution. An interrupt request happened when a PWM cycle completed.

The MSB of AUD_DH is signed bit, '0' for positive, '1' for negative. PWM output frequency (sample rate) is fixed at 32KHz. PWM data registers are AUD_DM, AUD_DH. The AUL_DM is low nibble (D3 ~ D0). AUD_DH is high nibble (D7 ~ D4). D7 is the signed bit and D6 ~ D0 is the length (clock number) of output active pulse. Software should write AUD_DM and AUD_DH before enable PWM.

When an interrupt request happened, PWM interrupt flag bit PWFG of STATUS register will be "1". The PWM will load previously-written-data into actual conversion port on end of a PWM code output. So program can write data into PWM data store safely at beginning of an interrupt service routine. (A PWM interrupt means PWM data loaded, next data is expected). This timing shall be controlled carefully such that data writing in the beginning of interrupt service routine is safe. If data is not changed during a conversion, previous data will be used.

This PWM output can drive 8 ohm speaker. PWM can be enabled or disabled by setting/clearing ENPWM of SYS0. When disabled, the PWMP, PWMN pins are all '0'. "HALT" instruction will disable PWM (clear ENPWM of SYS0) and the PWMP and PWMN pins will be tri-state.

5.9.2 10-Bits PWM/DAC

The frequency of PWM clock is fixed at 32 KHz if 10-bits PWM mode is selected by option. The 10-bits PWM data (AUD_DH[3:0], AUD_DM[3:0], AUD_DL[3:2]) are consist of AUD_DH, AUD_DM, AUD_DL three registers shown above. The data rage is 0 ~511. Software should write these registers before PWM is enabled. The other features of 10-bits PWM is the same as 8-bits PWM.

5.9.3 12-Bits PWM/DAC

The frequency of PWM clock is fixed at 32 KHz if 12-bits PWM mode is selected by option "PWM12S".The 12-bits PWM data (AUD_DH[3:0], AUD_DM[3:0], AUD_DL[3:0]) are consist of AUD_DH, AUD_DM, AUD_DL three registers shown above. The data rage is 0 ~2047. Software should write these registers before PWM is enabled. The other features of 12-bits PWM is the same as 8-bits PWM.

5.10 Reset Function

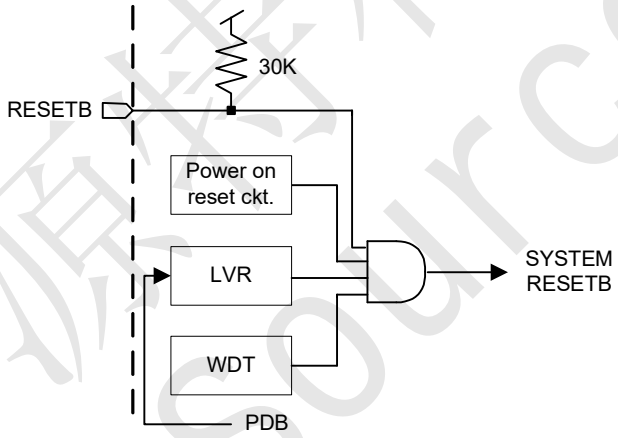


Figure 3: Reset structure

The system reset is come from four signals which are **Power on reset**, **Low voltage reset(LVR)**, **External RESETB pin** and **WDT overflow reset**.

Some reset input pins, PB3 and PC3, can be provided to reset this chip according to your option. These pins have 30K Ohm pull up resistor. For normal operation of this chip, a good reset is needed. The operation frequency of MCU will go back to normal mode when reset occurred in HALT mode.

5.11 System Clock Oscillator

This chip MCU is typically operated on 8.192MHz which is generated from internal RC oscillator 32MHz.

5.12 I/O Ports

There are totally four I/O ports, PA3~PA0, PB3~PB0, PD3~PD0 and PE3~PE0, whose input/output direction are defined by IOC_PA, IOC_PB, IOC_PD and IOC_PE.

PE3~PE0 are input or input/output direction defined by IOC_PE be selected by option. The wake-up functions of PA3~PA0, PB3~PB0, PD3~PD0 and PE3~PE0 are enabled or disabled by option. Their 1M/50K Ohm pull down resistors are optional.
In order to achieve touch function, CST & CSTM series support 220K Ohm pull down resistors. These resistors can be enabled by using 50K Ohm pull down resistor registers after "PD220K" is enabled. The 220K Ohm resistance value is almost fixed value when VCC change from 2.0V to 5.5V.
All I/O ports provides rising or falling edge wake up function. This double edge wake up function can be enabled by "BIWK" option.

5.12.1 Port PA (input/output)

The Port A are 4-bits bidirectional I/O ports. Their directions can be defined by IOC_PA bit by bit.
The following table describe the SFRs associated with Port A:

Symbol	Addr	R/W type	Reset	D3	D2	D1	D0	Description
IOC_PA	02H	R/W	0000	**IOCA3**	**IOCA2**	**IOCA1**	**IOCA0**	**"1" = output, "0" = input of related PA bit.**
DATA_PA	03H	R/W	xxxx	**DPA3**	**DPA2**	**DPA1**	**DPA0**	**Read from Port A input port and write to output port.**

Table 13: SFRs of Ports PA

In output mode, the data can be written out to external pin, and reading this output port will read the data internal latch. Pull-down resistor will be disabled when output mode is selected.
In input mode, Port A and Port B data can be read from external pin, and they are attached with 1M/50K Ohm pull-down resistor or not according to the options.

In addition, each pin of Port A and Port B also can be accompanied with wake-up function according to the options. In HALT mode, if some bits of Port A or Port B are accompanied with wake-up function, any rising edge occurred on that pin will wake up system and turn on oscillator, and the program counter of MCU will jump to the address $004H. This device will start to execute the wake-up sub-routing.

PA3 is provided with 38KHz modulator
I/O port PA3 built-in a 38KHz modulator combined with register DATA_PA bit-3, this function is enabled by **"F38K" option**. If F38K option is enabled, I/O port PA3 will output 38KHz clock signal when PA3 is configured as output port and DATA_PA bit-3 = 1. PA3 output low when PA3 is configured as output port and DATA_PA bit-3 = 0.
Notice: The PA3 output pad will be forced to low state automatically by hardware control when in halt mode for avoid external IR LED destroyed. Besides, the F38K option disabled, PA3 is a normal I/O port.

PA0 is provided with an analog input (Schmitt) for wake-up control
PA0 supports an analog input buffer with Schmitt circuit, it is enabled by "**RCWK" option** and supports low power consumption in halt mode, if PA0 analog signal keep about 0.5*VCC, so this function is suitable for recycle wakeup MCU by external RC time constant, external RC time constant is easy built by VCC connected to R and serial with C to VSS.
The block diagram and electrical characteristic of PA0 analog input buffer shown below. It takes about 5uA when PA0 input signal is 2.5v @VCC=5V in halt mode, otherwise, it takes about 500uA current if RCWK option disabled. This block function is enabled when RCWK option enabled by hardware after power on reset.

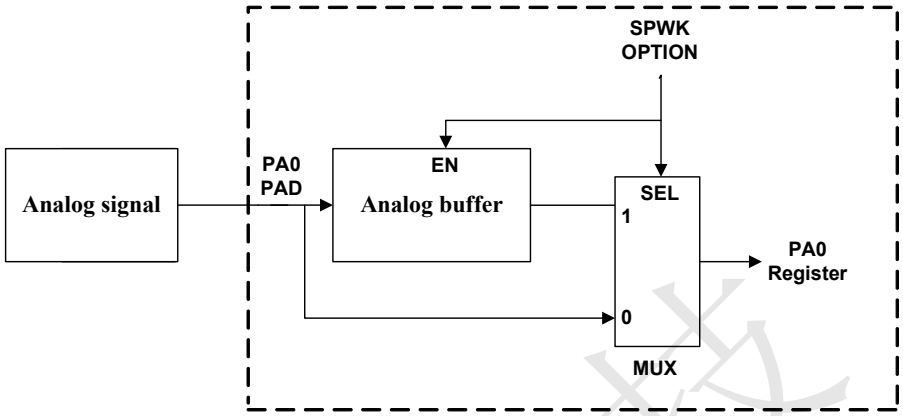


Figure 4. PA0 analog input structure

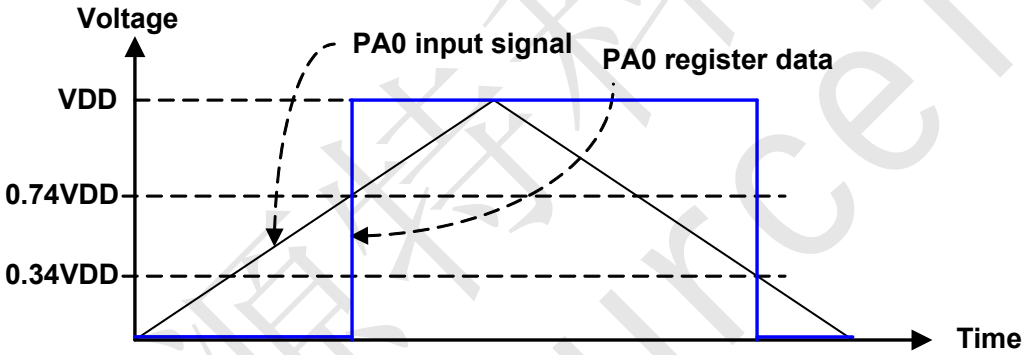


Figure 5. PA0 input signal and PA0 register data

5.12.2 Port PB (input/output)

The Port B are 4-bit bidirectional I/O ports. Their directions can be defined by IOC_PB bit by bit.

The following table describe the SFRs associated with Port B.

Symbol	Addr	R/W type	Reset	D3	D2	D1	D0	Description
IOC_PB	05H	R/W	0000	IOCB3	IOCB2	IOCB1	IOCB0	**"1" = output, "0" = input of related PB bit.**
DATA_PB	06H	R/W	xxxx	DPB3	DPB2	DPB1	DPB0	**Read from Port B input port and write to output port.**

Table 14: SFRs of Ports PB

In output mode, the data can be written out to external pin, and reading this output port will read the data internal latch. Pull-down resistor will be disabled when output mode is selected.
In input mode, Port B data can be read from external pin, and they are attached with 1M/50K Ohm pull-down resistor or not according to the options.

In addition, each pin of Port B also can be accompanied with wake-up function according to the options.
In HALT mode, if some bits of Port B are accompanied with wake-up function, any rising edge occurred on that pin will wake-up system and turn on oscillator, and the program counter of MCU will jump to the address $004H. This device will start to execute the wake-up sub-routing.

5.12.3 Port PC (output)

The Port C is 4-bits output port only.
Note: Port PC functions are not provided in CST5171S1.

The following table describe the SFRs associated with Port C.

Symbol	Addr	R/W type	Reset	D3	D2	D1	D0	Description
DATA_PC	04H	R/W	0000	DPC3	DPC2	DPC1	DPC0	Port C is output port only. Write to Port C output port.

Table 15: SFR of Port PC

5.12.4 Port PD (input/output)

Whether all 4-bits of the Port D are input or output ports depends on IOC_PD control register. They are accompanied with 1M/50K Ohm pull-down resistor or not according to the options if they are in the input mode.

The following table describe the SFRs associated with Port D.

Symbol	Addr	R/W type	Reset	D3	D2	D1	D0	Description
IOC_PD	0CH	R/W	0000	IOCD3	IOCD2	IOCD1	IOCD0	"1" = output, "0" = input of related PD bit.
DATA_PD	0DH	R/W	xxxx	DPD3	DPD2	DPD1	DPD0	Read from Port D input port and write to output port.

Table 16: SFRs of Port PD

5.12.5 Port PE (input) Selected by option "PEIO=0".

All 4-bits of the Port E are input ports only. They are accompanied with 1M/50K Ohm pull-down resistor or not according to the options.

The following table describe the SFRs associated with Port E.

Symbol	Addr	R/W type	Reset	D3	D2	D1	D0	Description
DATA_PE	0EH	R/W	xxxx	DPE3	DPE2	DPE1	DPE0	Port E defined as I/O port or input port depends on option PEIO. Read from Port E input port and write to output port.

Table 17: SFR of Port PE input port only

5.12.6 Port PE (input/output) Selected by option "PEIO=1".

Whether all 4-bits of the Port E are input or output ports depends on IOC_PE control register. They are accompanied with 1M/50K Ohm pull-down resistor or not according to the options if they are in the input mode.

The following table describe the SFRs associated with Port CE.

Symbol	Addr	R/W type	Reset	D3	D2	D1	D0	Description
IOC_PE	01H	R/W	0000	IOCE3	IOCE2	IOCE1	IOCE0	Enable when option "PEIO" selected. "1" = output, "0" = input of related PE bit.
DATA_PE	0EH	R/W	xxxx	DPE3	DPE2	DPE1	DPE0	Port E defined as I/O port or input port depends on option PEIO. Read from Port E input port and write to output port.

Table 18: SFR of Port PE input/output port

There are three modes on Port E I/O mode. They are single OP mode, two comparators mode and comparator & OP mode shown in table below:

Item	Port E Structure	Relative Options	Reference Figure
Mode 1	Single OP mode	OPEN	Figure 6
Mode 2	Two comparators mode	CMPEN1、CMPEN2、B1RZ、B3RZ	Figure 7
Mode 3	Comparator & OP mode	CMPEN1、OPEN、B1RZ	Figure 8

Table 19: Structure of PE

These three modes can be enabled by option OPEN, CMPEN1 and CMPEN2. Option B1RZ is used for reading control DATA_PE1. If B1RZ is enabled, DATA_PE1 will read always 0. Otherwise, it will read the state of external Port PE1. Another option B3RZ is the same function as B1RZ. Option B3RZ is used for reading control DATA_PE3.

Notice: Only CST series provided OP function.

Mode1. Single OP mode

Port E provides one OP, if option OPEN is enabled. In this mode, the positive, negative input and output pin of OP is configured as below. In order to avoid interference between PE1 and PE2 pin, it's recommended PE1 must be set as input port.

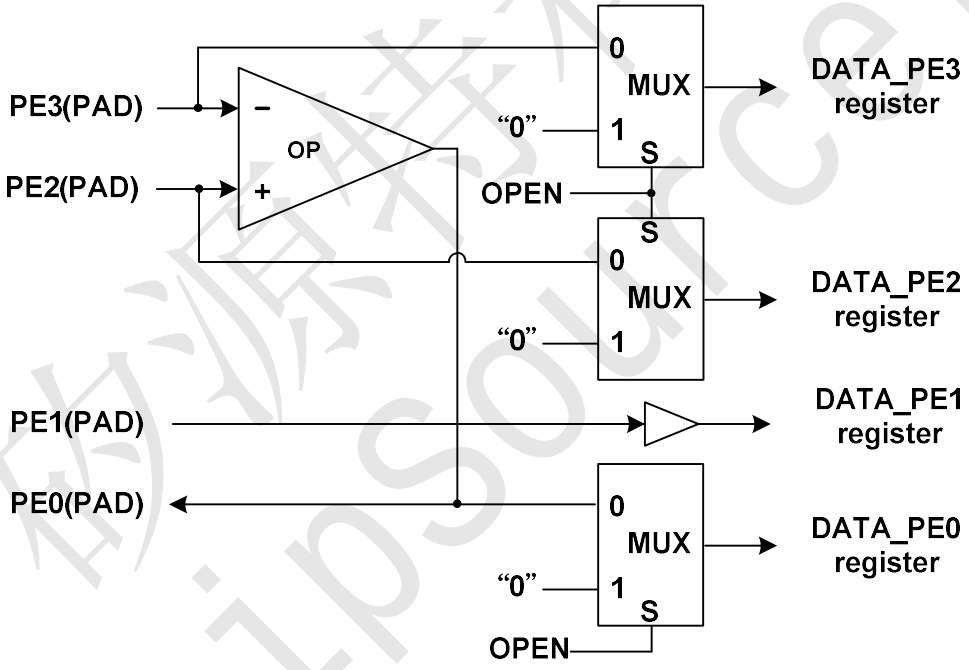


Figure 6. Port E mode 1 block diagram

Mode2. Two comparators mode

Port PE provides two comparators if option CMPEN1 and CMPEN2 are enabled. One of them may be enabled by individual option. In this mode, the positive and negative input of comparator is configured as below.

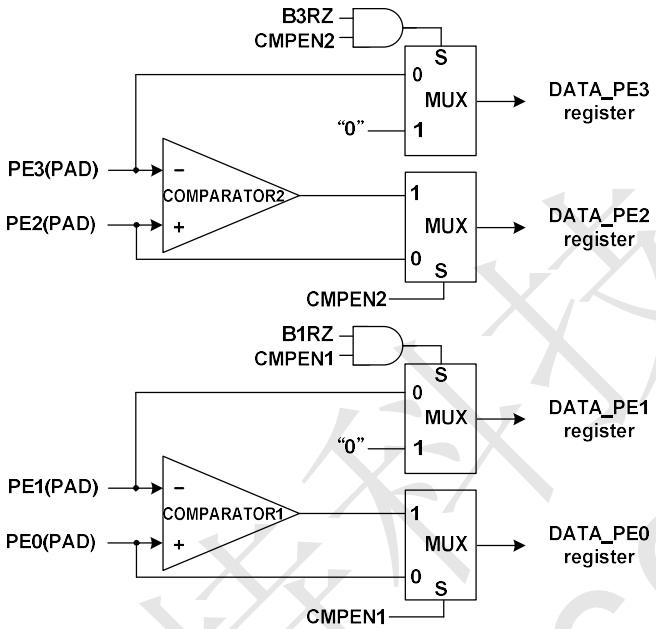


Figure 7. Port E mode 2 block diagram

Option B1RZ is used for reading control DATA_PE1. If B1RZ is enabled, DATA_PE1 will read always 0. Otherwise, it will read the state of external Port PE1. Another option B3RZ is the same function as B1RZ. Option B3RZ is used for reading control DATA_PE3. The option B1RZ & B3RZ configuration as shown below.

Option CMPEN1 & B1RZ configuration

CMPEN1	CMPEN2 & OPEN	B1RZ	Reading DATA_PE1~0
0	0	X	Port E is pure I/O port
1	0	0	Reading DATA_PE1 register comes from the PE1 external Port Reading DATA_PE0 register comes from the output of comparator1
1	0	1	Reading DATA_PE1 register is always 0 Reading DATA_PE0 register comes from the output of comparator1

Table 20. Port E comparator1 configuration

Option CMPEN2 & B3RZ configuration

CMPEN2	CMPEN1 & OPEN	B3RZ	Reading DATA_PE3~2
0	0	X	Port E is pure I/O port
1	0	0	Reading DATA_PE3 register comes from the PE3 external Port Reading DATA_PE2 register comes from the output of comparator2
1	0	1	Reading DATA_PE3 register is always 0 Reading DATA_PE2 register comes from the output of comparator2

Table 21. Port PCE comparator2 configuration

Mode3. Comparator and OP mode

Port E provides comparator and OP mode if option CMPEN1 and OPEN are enabled. Option CMPEN2 must be disabled. In this mode, the comparator and OP is configured as below. It's suitable for small signal detected used on remote toy car applications.

Notice: Only CST series provided OP function.

Option OPEN, CMPEN1 & B1RZ configuration

OPEN	CMPEN1	CMPEN2	B1RZ	Reading DATA_PE3~0
0	0	0	x	Port E is pure I/O port
1	1	0	0	Reading DATA_PE2 or DATA_PE3 register is always 0 Reading DATA_PE1 register comes from the PE1 external Port Reading DATA_PE0 register comes from the output of comparator1
1	1	0	1	Reading DATA_PE2 or DATA_PE3 register is always 0 Reading DATA_PE1 register is always 0 Reading DATA_PE0 register comes from the output of comparator1

Table 22. Port PE option B1RZ configuration

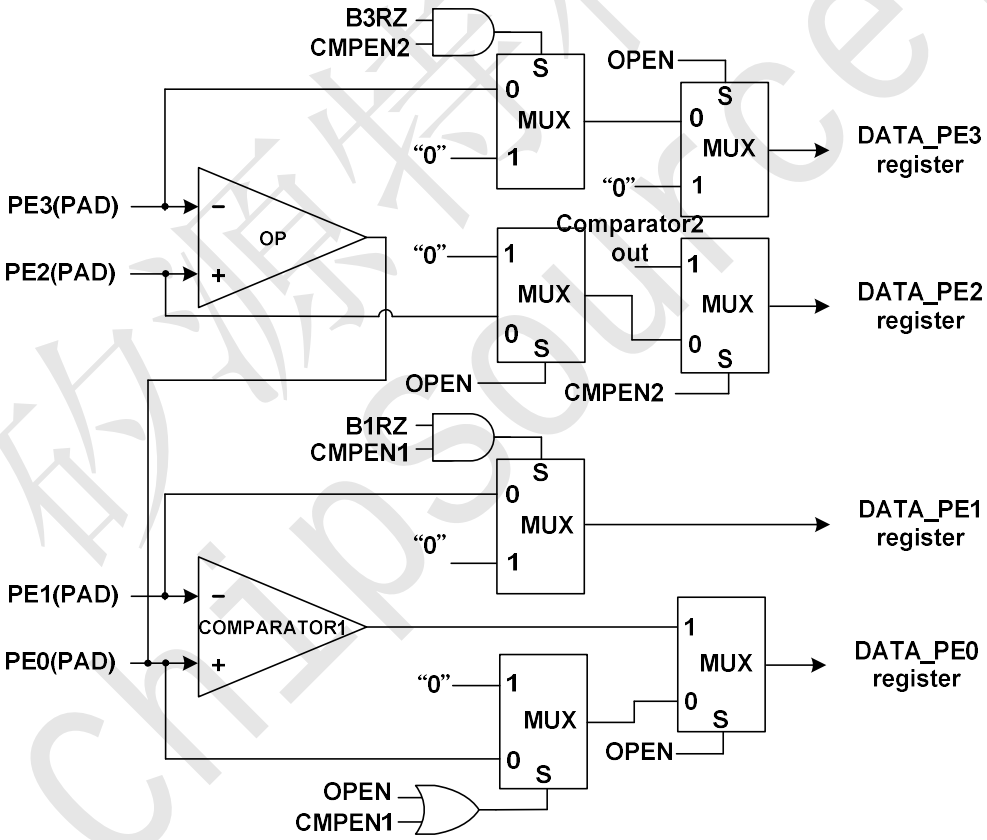


Figure 8. Port E mode 3 block diagram

6. CST5182A/5171A/5171S1/5086A The Application Circuit

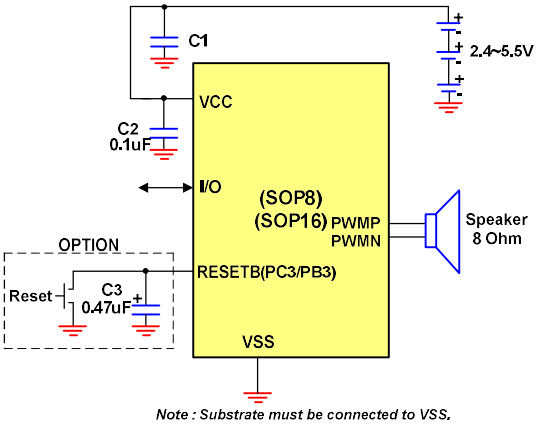


Figure 9. PWM Applications circuit -1

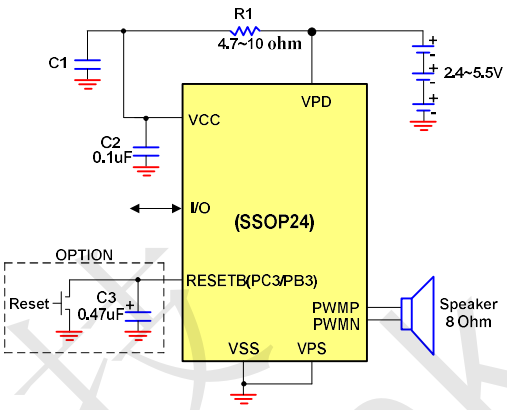


Figure 10. PWM Applications circuit -2

DAC Selected by option

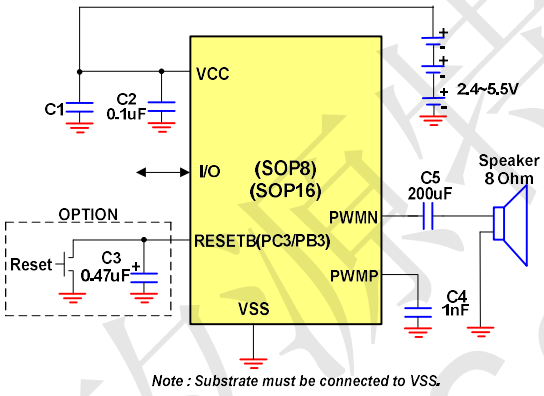


Figure 11. DAC Applications circuit -1

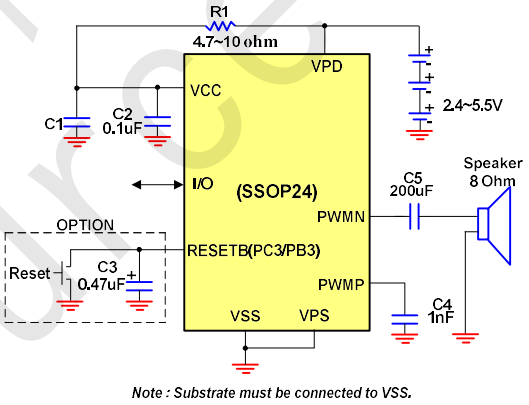


Figure 12. DAC Applications circuit -2

Notice:

1. **Regarding recording or remote car applications, please reference application note on web site.**
2. **C1 : 47 uF ~ 100 uF(depends on applications), C2：0.1 uF**
3. **DAC Applications, please reference application note on web site.**

7. CST5182A/5171A/5171S1/5086A Option Registers table

Option Name	Function Description
RCWK	Enable PA0 RC wakeup.
PWM64K	Enable PWM int. freq. 64KHz.
ENDAC	Enable DAC function.
WAKEBA	Wake-up enable for PA3~PA0 respectively.
WAKEBB	Wake-up enable for PB3~PB0 respectively.
WAKEBD	Wake-up enable for PD3~PD0 respectively.
WAKEBE	Wake up enable for PE3~PE0 respectively.
PD50KPA	50K Ohm pull down resistor for PA3~PA0 respectively.
PD50KPB	50K Ohm pull down resistor for PB3~PB0 respectively.
PD50KPD	50K Ohm pull down resistor for PD3~PD0 respectively.
PD50KPE	50K Ohm pull down resistor for PE3~PE0 respectively.
PD1MPA	1M Ohm pull down resistor for PA3~PA0 respectively.
PD1MPB	1M Ohm pull down resistor for PB3~PB0 respectively.
PD1MPD	1M Ohm pull down resistor for PD3~PD0 respectively.
PD1MPE	1M Ohm pull down resistor for PE3~PE0 respectively.
FHC	Force output high of PC3~PC0 respectively.
FHD	Force output high of PD3~PD0 respectively.
RSTBPB3	PB3 external reset pin function.
RSTBPC3	PC3 external reset pin function.
WDENB	Watch dog timer function.
PDENB	Enable HALT mode function.
ENOP	OPA function @ PE3(in-),PE2(in+),PE0(out).
PD220K	Change 50K Ohm pull-down resistor to 220K Ohm.
CMP #2	Comparator #2 function.
CMP #1	Comparator #1 function.
PWM12S	Enable PWM 12-bits function.
PWM10S	Enable PWM 10/8-bits function.
LOPENC	Output weak low for PC3~PC0.
LOPEND	Output weak low for PD3~PD0.
SECUOPT	Security control.
F38K	PA3 38KHz output function.
BIWK	Enable bi-directional wake-up function.
OPTADJ	Enable OSC internal adjustment (IADJ) function.
PEIO	Enable Port E I/O function.
DRV4MA	Driving capacity 4mA/20mA of output port,
B3RZ	PE3 mode select when CMP enable, '1'=PE3 will be read as zero, '0'=The read values of PE3 will be the data on pad.
B1RZ	PE1 mode select when CMP enable, '1'=PE1 will be read as zero, '0'=The read values of PE1 will be the data on pad.

8. CST5182A/5171A/5171S1/5086A The Revision History

Version	Description	Page	Date
1.0	Established		2020-04-29
1.1	Operating voltage 2.0V~5.5V	1, 6	2020-05-29
1.2	Added CST5182A description	1-5, 7-8, 10	2020-11-16
1.3	Added CST5171S1 description Added Wake-up time-constant	1-2, 7, 16 6	2021-03-22
1.4	Modify CST5171S1 description	2	2021-12-

24 Table 23: Revision History