3Walts Mono Filter-free Class-D Audio Power Amplifier

General Description

The LPA2104 is a high efficiency, 3.0W mono class-D audio power amplifier. A new developed filterless PWM modulation architecture further reduces EMI and THD+N, as well as eliminates the LC output filter, reducing external component count, sys cost, and simplifying design.

Operating in a single 5V supply, LPA2104 is capable of driving 4Ω speaker load at a continuous average output of 3.05W/10% THD+N or 2.6W/1% THD+N. The LPA2104 has high efficiency with speaker load compared to a typical class D amplifier. With a 3.6V supply driving an 8Ω speaker , the efficiency for a 400mW power level is 90%.In cellular handsets, the earpiece, speaker phone, and melody ringer can each be driven by the LPA2104. The gain of LPA2104 is externally configurable which allows independent gain control from multiple sources by summing signals from separate sources.

The LPA2104 is available in space-saving SOP8 and MSOP8 Packaging packages.

Order Information

LPA2104 □ □ □

F: Pb-Free

Package Type
SO: SOP8
MS: MSOP8

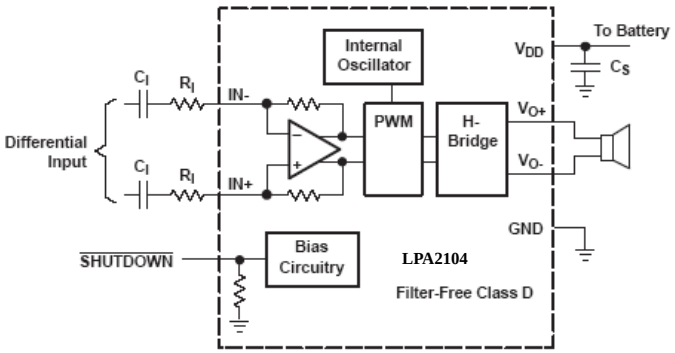
Applications

- PMP,PSP, Game, Data-Bank
- Cellular and Smart mobile phone
- PDA/DSC

Features

- Unique Modulation Scheme Reduces EMI Emissions
- Efficiency at 3.6V With an 8-Ω Speaker:
  - – 90% at 400 mW
  - – 82% at 100 mW
- Low 2.5mA Quiescent Current
- 0.5μA Shutdown Current
- 2.5V to 6V Wide Supply Voltage
- Shutdown Pin has 1.8V Compatible Thresholds
- Optimized PWM Output Stage Eliminates LC Output Filter
- Improved PSRR (−80 dB) Eliminates Need for a Voltage Regulator
- Fully Differential Design Reduces RF Rectification
- and Eliminates Bypass Capacitor
- Improved CMRR Eliminates Two Input Coupling Capacitors
- Internally Generated 750kHz Switching Frequency
- Integrated Pop and Click Suppression Circuitry
- SOP8 and MSOP8 Packaging
- RoHS compliant and 100% lead(Pb)-free

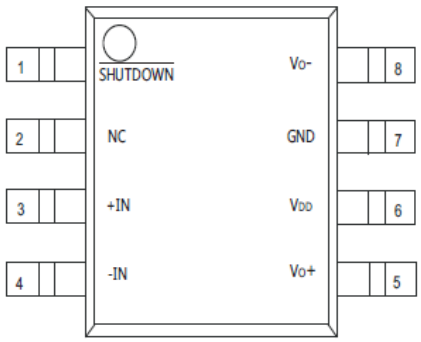
Typical Application Circuit



Marking Information

Please see website:
www.lowpowersemi.com/LPA2104

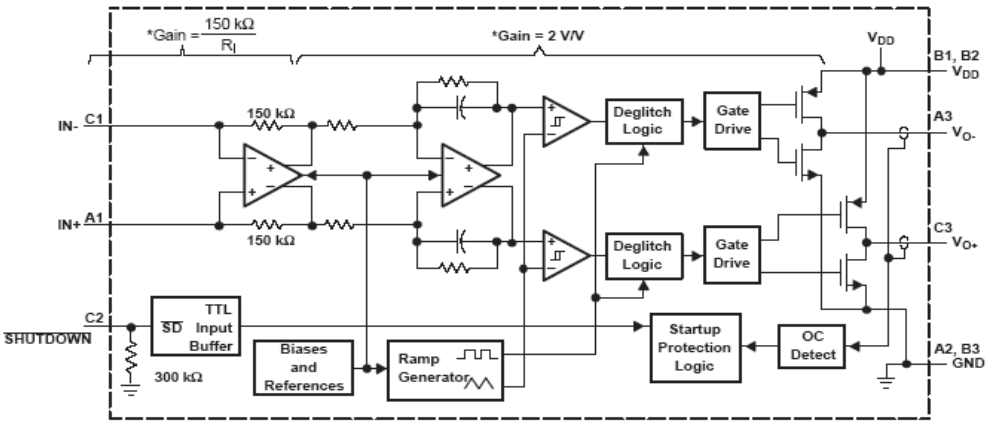
Functional Pin Description

Package Type	Pin Configurations
SOP8/MSOP8	

Pin Description

Pin	PIN No	DESCRIPTION
SHUTDOWN	1	Shutdown terminal (active low logic)
NC	2	No Connecter
+IN	3	Positive differential input
-IN	4	Negative differential input
VO+	5	Negative BTL output
VDD	6	Power supply.
GND	7	High-current ground
VO-	8	Positive BTL output

Function Block Diagram



Absolute Maximum Ratings

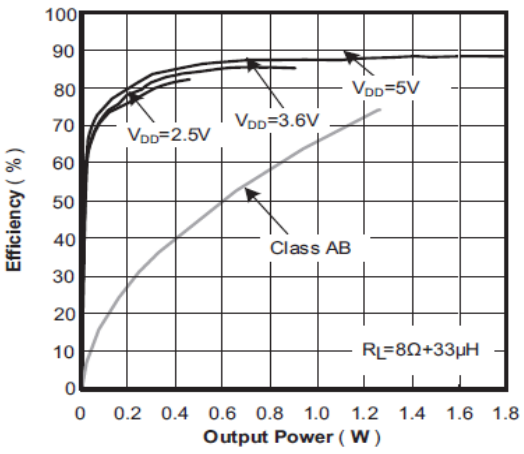
- ✧ Input Voltage to GND (V_{INA}, V_{INB}) ---------- 6V
- ✧ Adapter Voltage to GND (V_{ADP}) ----------0.3V to 6V
- ✧ Supply Voltage, V_{DD} ---------- -0.3 V to 6V
- ✧ Voltage at Any Input Pin ---------- -0.3 V to V_{DD} +0.3
- ✧ Junction Temperature, T_{JMAX} ---------- 150°C
- ✧ Storage Temperature Rang, T_{stg} ---------- -65°C to 150°C
- ✧ ESD Susceptibility ---------- 2kV
- ✧ Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ---------- 260°C
- ✧ Thermal Resistance θ_{JA} (WCSP) ---------- 77°C/W

Electrical Characteristics

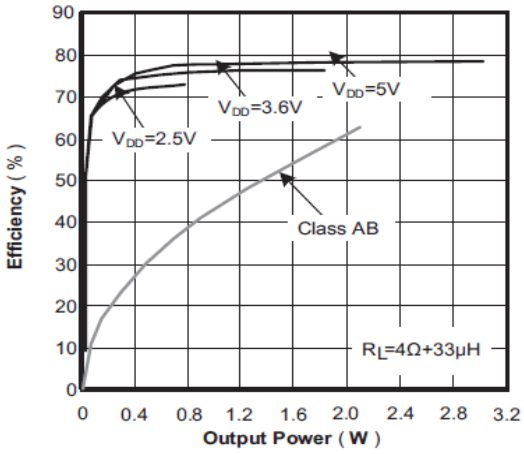
Symbol	Parameter	Conditions		LPA2104 Min.	LPA2104 Typ.	LPA2104 Max.	Unit
V_{OS}	Output offset voltage (measured differentially)	Vi=0V,Av=2V/V,VDD=2.5V to 5.5V			1	25	mV
PSRR	Power supply rejection ration	V_{DD}=2.5V to 5.5V			-72	-55	dB
CMRR	Common mode rejection ratio	VDD=2.5V to 5.5V,Vic=VDD/2 to 0.5V,Vin=VDd/2 to Vdd-0.8V			-60	-48	dB
I_{IH}	High-level input current	V_{DD}=5.5V, Vi=5.8V				100	uA
I_{IL}	Low-level input current	V_{DD}=5.5V, Vi=-0.3V				5	uA
I_Q	Quiescent current	V_{DD}=5.5V, no load			3.52		mA
		V_{DD}=3.6V, no load			2.40		
		V_{DD}=2.5V, no load			2.06		
I_{SHDN}	Shutdown Current	V_{SHDN}=0.35V, V_{DD}=2.5V to 5.5V			0.5		μA
I_{LIM}	P-Channel Current Limit			1.2			A
$R_{DS(ON)}$	Static drain-source on-state resistance	V_{DD}=5.5V, no load			400		m Ω
		V_{DD}=3.6V, no load			500		
		V_{DD}=2.5V, no load			700		
](SW)	Switching frequency	V_{DD}=2.5V to 5.5V			750		KHz
Gain		VDD=2.5 to 5.5V			$\frac{300\ k\Omega}{R_I}$		V/V
P_O	Output power	THD+N=10%, F=1KHz,R_L=4 Ω	V_{DD}=5.0V		3.05		W
			V_{DD}=3.6V		1.28		
			V_{DD}=2.5V		0.64		
		THD+N=1%, F=1KHz,R_L=4 Ω	V_{DD}=5.0V		2.6		W
			V_{DD}=3.6V		1.06		
			V_{DD}=2.5V		0.46		
		THD+N=10%, F=1KHz,R_L=8 Ω	V_{DD}=5.0V		1.7		W
			V_{DD}=3.6V		0.79		
			V_{DD}=2.5V		0.39		
		THD+N=1%, F=1KHz,R_L=8 Ω	V_{DD}=5.0V		1.36		W
			V_{DD}=3.6V		0.64		
			V_{DD}=2.5V		0.32		
THD+N	Total harmonic distortion plus noise	V_{DD}=5V,,Po=1W,RL=8 Ω f=1KHz		0.123			%
		V_{DD}=3.6V,,Po=0.5W,RL=8 Ω f=1KHz		0.130			
		V_{DD}=2.5V,,Po=0.2W,RL=8 Ω f=1KHz		0.163			
kSVR	Supply ripple rejection ratio	V_{DD}=3.6V,Inputs ac-grounded with Ci=2uF	F=217Hz,V9ripple) =200mVpp		-70		dB
CMRR	Common mode rejection ratio	VDD=3.6V, Vic=1Vpp	F=217Hz		-80		dB
Zt	Start-up time from shutdown	VDD=3.6			40		mS

Typical Operating Characteristics

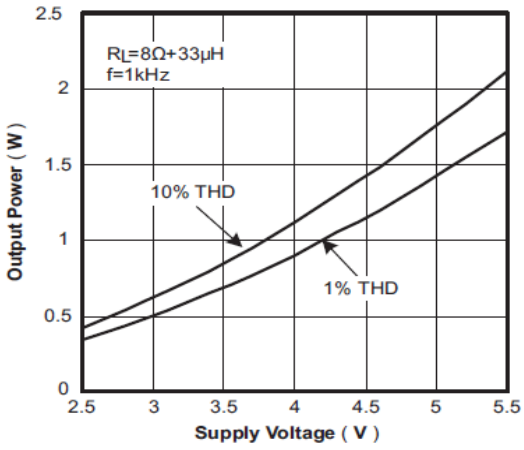
EFFICIENCY vs OUTPUT POWER



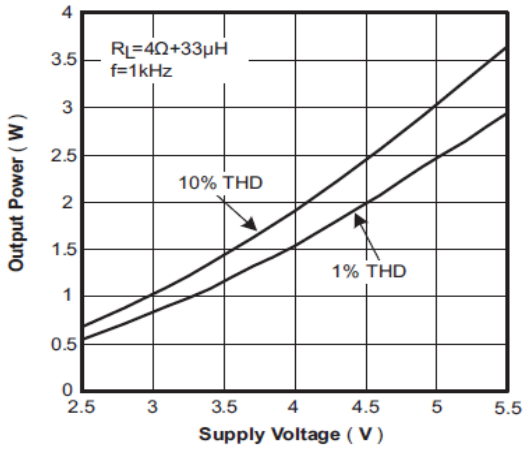
EFFICIENCY vs OUTPUT POWER



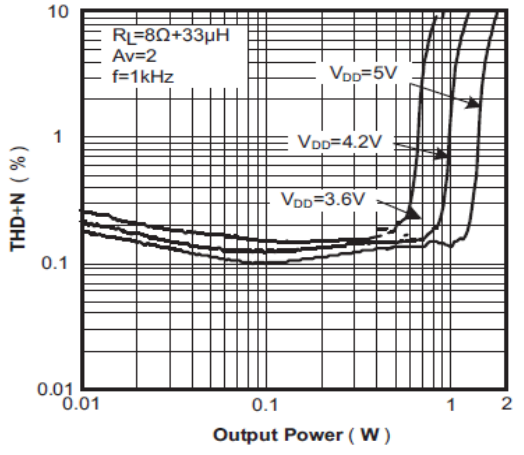
OUTPUT POWER vs SUPPLY VOLTAGE



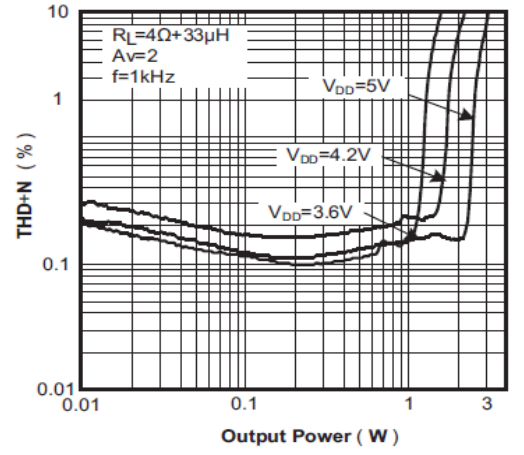
OUTPUT POWER vs SUPPLY VOLTAGE



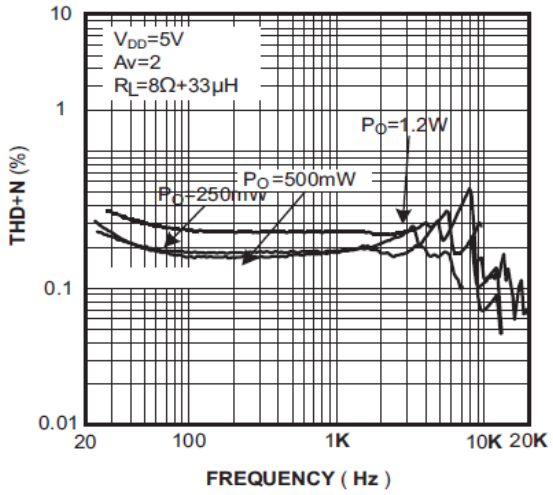
THD+N vs OUTPUT POWER



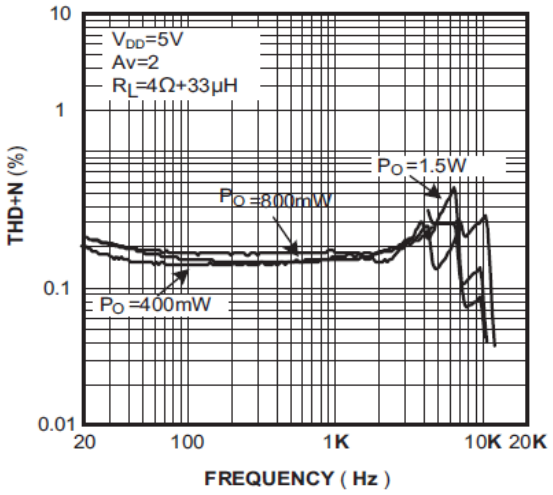
THD+N vs OUTPUT POWER



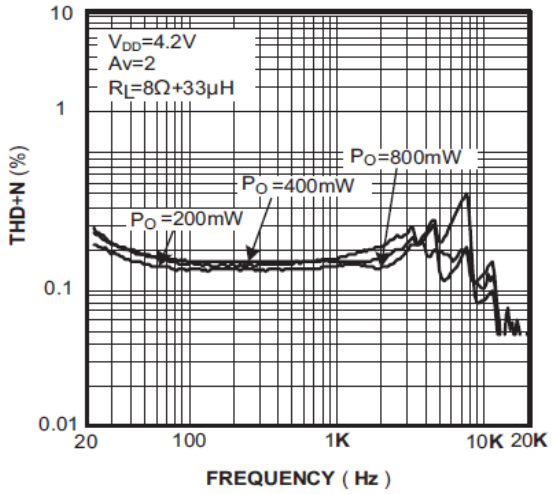
THD+N vs FREQUENCY



THD+N vs FREQUENCY



THD+N vs FREQUENCY



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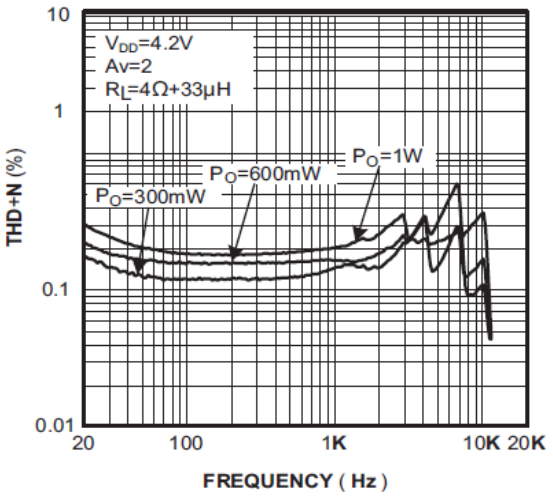
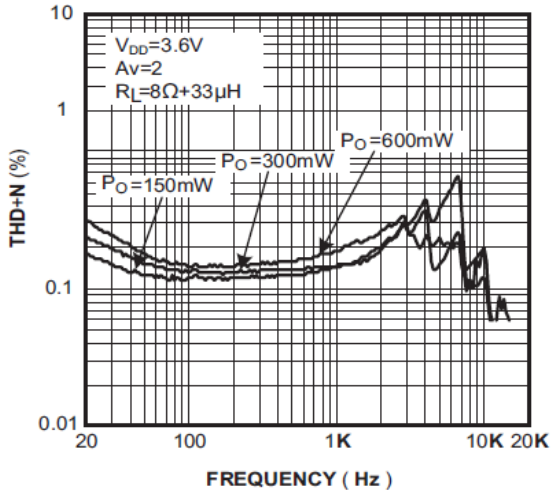
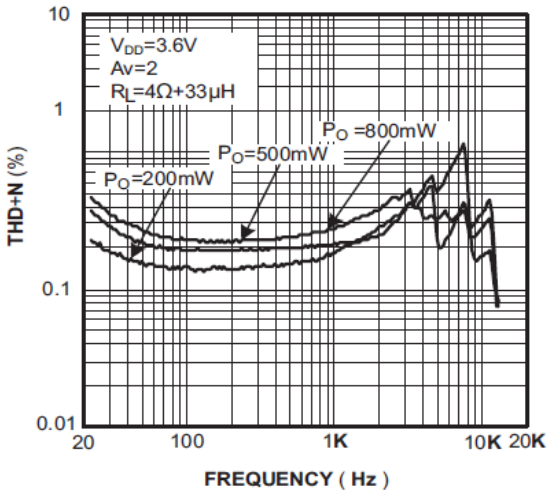


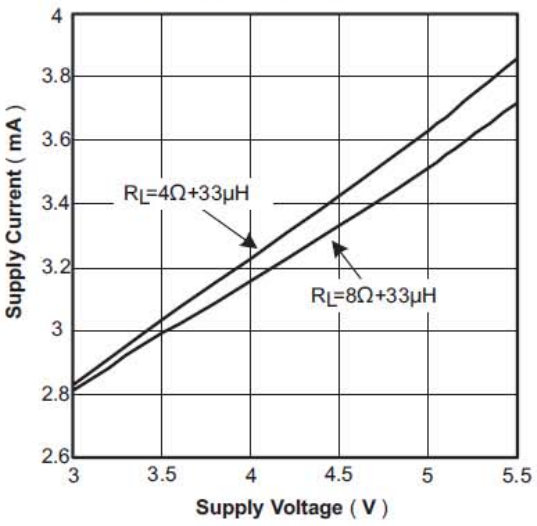
THD+N vs FREQUENCY



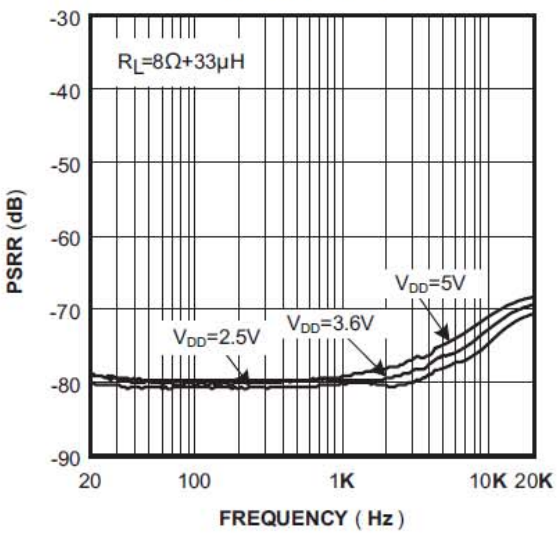
THD+N vs FREQUENCY



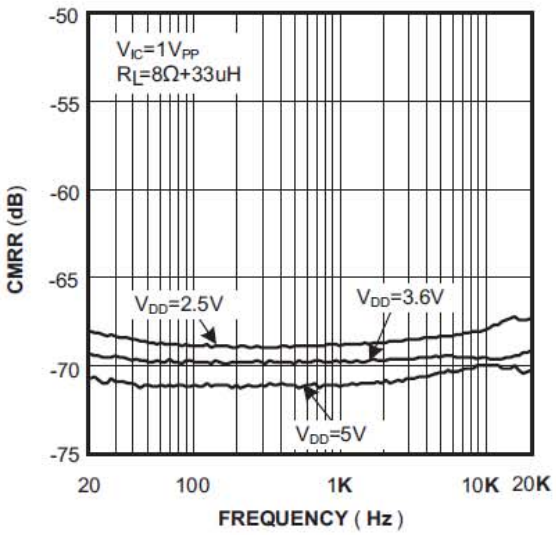
SUPPLY CURRENT vs SUPPLY VOLTAGE



PSRR vs FREQUENCY



CMRR vs FREQUENCY



Application Information

The LPA2104 is a fully differential amplifier with differential inputs and outputs. The fully differential amplifier consists of a differential amplifier and a common-mode amplifier. The differential amplifier ensures that the amplifier outputs a differential voltage on the output that is equal to the differential input times the gain. The common-mode feedback ensures that the common-mode voltage at the output is biased around VDD/2 regardless of the common-mode voltage at the input. The fully differential LPA2104 can still be used with a single-ended input; however, the LPA2104 should be used with differential inputs when in a noisy environment, like a wireless handset, to ensure maximum noise rejection.

Advantages of Fully Differential Amplifiers

Input-coupling capacitors not required:

The fully differential amplifier allows the inputs to be biased at voltage other than mid-supply. For example, if a codec has a mid-supply lower than the mid-supply of the LPA2104, the common-mode feedback circuit will adjust, and the LPA2104 outputs will still be biased at mid-supply of the LPA2104. The inputs of the LPA2104 can be biased from 0.5V toVDD-0.8 V. If the inputs are biased outside of that range, input-coupling capacitors are required.

Mid-supply bypass capacitor, C(BYPASS), not required:

- The fully differential amplifier does not require a bypass capacitor. This is because any shift in the mid-supply affects both positive and negative channels equally and cancels at the differential output.

Better RF−immunity:

-GSM handsets save power by turning on and shutting off the RF transmitter at a rate of 217Hz.The transmitted signal is picked-up on input and output traces. The fully differential amplifier cancels the signal much better than the typical audio amplifier.

Component Selection

Figure 30 shows the LPA2104 typical schematic with differential inputs and Figure 31 shows the LPA2104 with differential inputs and input capacitors, and Figure 32 shows the LPA2104 with single-ended inputs. Differential inputs should be used whenever possible because the single-ended inputs are much more susceptible to noise.

REF DES	VALUE
R_I	150kΩ (±0.5%)
C_S	1μF (+22%,-80%)
C_I (1)	3.3nF (±10%)

(1) C_I is only needed for single-ended input or if V_{ICM} is not between 0.5 V and V_{DD} – 0.8 V. C_I = 3.3 nF (with R_I = 150 kΩ) gives a high-pass corner frequency of 321 Hz.

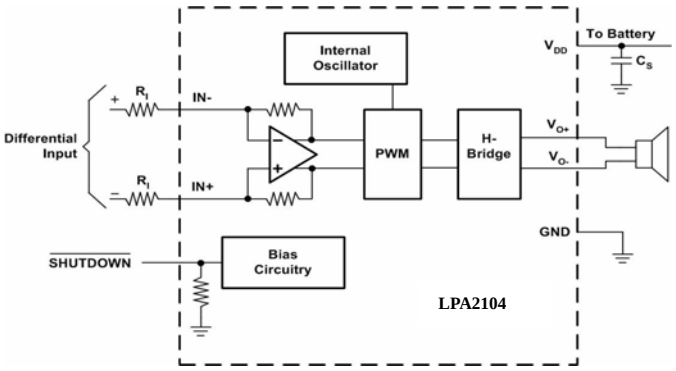


Figure 30. Typical Application Schematic With Differential Input for a Wireless Phone

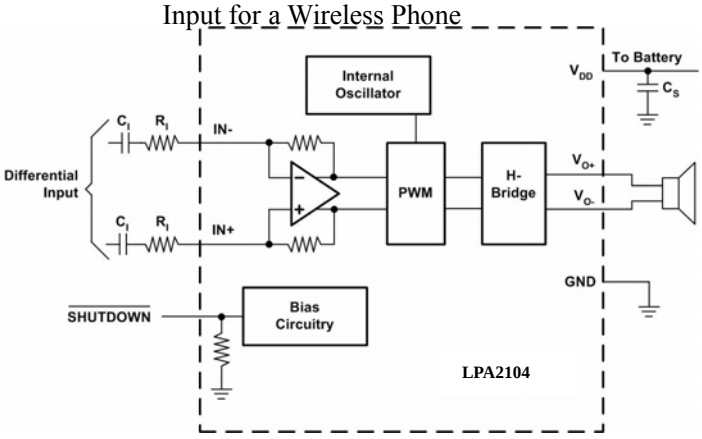


Figure 31. Typical Application Schematic With Differential Input and Input Capacitors

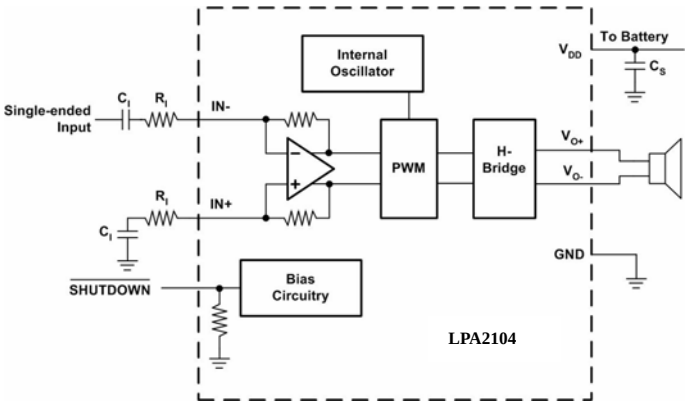


Figure 32. Typical Application Schematic With Single-Ended Input

Input Resistors (RI)

The input resistors (RI) set the gain of the amplifier according to equation (1).

$$\text{Gain} = \frac{2 \times 150\text{k}\Omega}{R_I} \left(\frac{V}{V}\right) \quad \text{----------(1)}$$

Resistor matching is very important in fully differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistors. CMRR, PSRR, and cancellation of the second harmonic distortion diminish if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance resistors or better to keep the performance optimized. Matching is more important than overall tolerance. Resistor arrays with 1%

matching can be used with a tolerance greater than 1%.
Place the input resistors very close to the LPA2104 to limit noise injection on the high-impedance nodes.
For optimal performance the gain should be set to 2 V/V or lower. Lower gain allows the LPA2104 to operate at its best, and keeps a high voltage at the input making the inputs less susceptible to noise.

Decoupling Capacitor (CS)

The LPA2104 is a high-performance class-D audio amplifier that requires adequate power supply decoupling to ensure the efficiency is high and total harmonic distortion (THD) is low. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1µF, placed as close as possible to the device VDD lead works best. Placing this decoupling capacitor close to the LPA2014 is very important for the efficiency of the class-D amplifier, because any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency. For filtering lower-frequency noise signals, a 1 0µF or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

Input Capacitors (CI)

The LPA2104 does not require input coupling capacitors if the design uses a differential source that is biased from 0.5 V to VDD – 0.8 V (shown in Figure 31). If the input signal is not biased within the recommended common –mode input range, if needing to use the input as a high pass filter (shown in Figure 32), or if using a single-ended source (shown in Figure 33), input coupling capacitors are required.
The input capacitors and input resistors form a high-pass filter with the corner frequency, fc, determined in equation (2).

$$f_c = \frac{1}{(2\pi R_I C_I)} \quad \text{----------(2)}$$

The value of the input capacitor is important to consider as it directly affects the bass (low frequency) performance of the circuit. Speakers in wireless phones cannot usually respond well to low frequencies, so the corner frequency can be set to block low frequencies in this application.Equation (3) is reconfigured to solve for the input coupling capacitance.

$$C_I = \frac{1}{(2\pi R_I f_c)} \quad \text{----------(3)}$$

If the corner frequency is within the audio band, the capacitors should have a tolerance of ± 10% or better, because any mismatch in capacitance causes an impedance mismatch at the corner frequency and below.
For a flat low-frequency response, use large input coupling capacitors (1 µF). However, in a GSM phone the ground signal is fluctuating at 217 Hz, but the signal from the codec does not have the same 217 Hz fluctuation. The difference between the two signals is amplified, sent to the speaker, and heard as a 217 Hz hum.

Summing Input Signals

Most wireless phones or PDAs need to sum signals at the audio power amplifier or just have two signal sources that need separate gain. The LPA2104 makes it easy to sum signals or use separate signal sources with different gains. Many phones now use the same speaker for the earpiece and ringer, where the wireless phone would require a much lower gain for the phone earpiece than for the ringer. PDAs and phones that have stereo headphones require summing of the right and left channels to output the stereo signal to the mono speaker.

Summing Two Differential Input Signals

Two extra resistors are needed for summing differential signals (a total of 5 components). The gain for each input source can be set independently (see equations (4) and(5), and Figure 33).

$$\text{Gain1} = \frac{V_O}{V_{I1}} = \frac{2 \times 150k\Omega}{R_{I1}} \left(\frac{V}{V}\right) \quad \text{----------(4)}$$

$$\text{Gain2} = \frac{V_O}{V_{I2}} = \frac{2 \times 150k\Omega}{R_{I2}} \left(\frac{V}{V}\right) \quad \text{----------(5)}$$

If summing left and right inputs with a gain of 1 V/V, use RI1 = RI2 = 300 k

If summing a ring tone and a phone signal, set the ring-tone gain to Gain 2 = 2 V/V, and the phone gain to Gain 1 = 0.1 V/V. The resistor values would be. . .
RI1=3M Ω , and=RI2=150k Ω

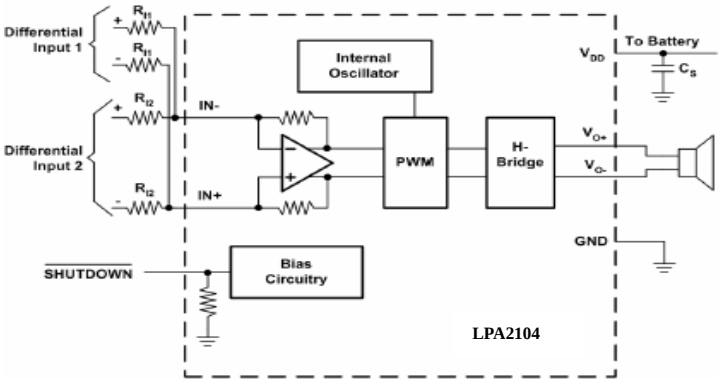


Figure 33. Application Schematic With Summing Two Differential Inputs

Summing Two Single-Ended Input Signals

Four resistors and three capacitors are needed for summing single-ended input signals. The gain and corner frequencies (fc 1 and fc2) for each input source can be set independently (see equations (9) through (12), and Figure 35). Resistor, RP, and capacitor, CP, are needed on the IN+ terminal to match the impedance on the IN– terminal. The single-ended inputs must be driven by low impedance sources even if one of the inputs is not outputting an ac signal.

$$Gain1 = \frac{V_O}{V_{I1}} = \frac{2 \times 150k\Omega}{R_{I1}} \left(\frac{V}{V}\right) \text{ ----------(9)}$$

$$Gain2 = \frac{V_O}{V_{I2}} = \frac{2 \times 150k\Omega}{R_{I2}} \left(\frac{V}{V}\right) \text{ ----------(10)}$$

$$C_{I1} = \frac{1}{(2\pi R_{I1} f_{c1})} \text{ ----------(11)}$$

$$C_{I2} = \frac{1}{(2\pi R_{I2} f_{c2})} \text{ ----------(12)}$$

$$CP = C_{I1} + C_{I2} \text{ ----------(13)}$$

$$R_P = \frac{R_{I1} \times R_{I2}}{(R_{I1} + R_{I2})} \text{ ---------- (14)}$$

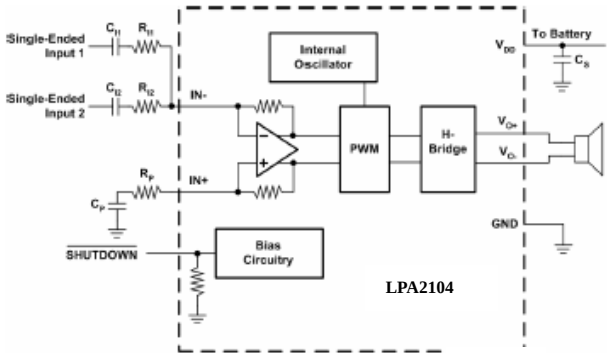


Figure 35. Application Schematic With EUA2011 Summing Two Single-Ended Input

Layout Considerations

As output power increases, interconnect resistance (PCB traces and wires) between the amplifier, load and power supply create a voltage drop. The voltage loss on the traces between the LPA2104 and the load results is lower output power and decreased efficiency. Higher trace resistance between the supply and the LPA2104 has the same effect as a poorly regulated supply, increase ripple on the supply line also reducing the peak output power. The effects of residual trace resistance increases as output current increases due to higher output power, decreased load impedance or both. To maintain the highest output voltage swing and corresponding peak output power, the PCB traces that connect the output pins to the load and the supply pins to the power supply should be as wide as possible to minimize trace resistance.

The use of power and ground planes will give the best THD+N performance. While reducing trace resistance, the use of power planes also creates parasite capacitors that help to filter the power supply line.

The inductive nature of the transducer load can also result in overshoot on one or both edges, clamped by the parasitic diodes to GND and $_{VDD}$ in each case. From an EMI stand- point, this is an aggressive waveform that can radiate or conduct to other components in the system and cause interference. It is essential to keep the power and output traces short and well shielded if possible. Use of ground planes, beads, and micro-strip layout techniques are all useful in preventing unwanted interference.

As the distance from the LPA2104 and the speaker increase, the amount of EMI radiation will increase since the output wires or traces acting as antenna become more efficient with length. What is acceptable EMI is highly application specific.

Ferrite chip inductors placed close to the LPA2104 may be needed to reduce EMI radiation. The value of the ferrite chip is very application specific.

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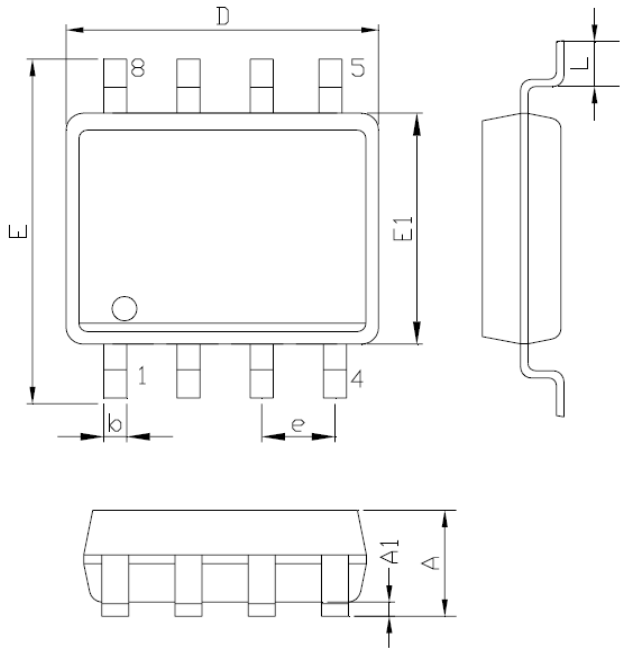
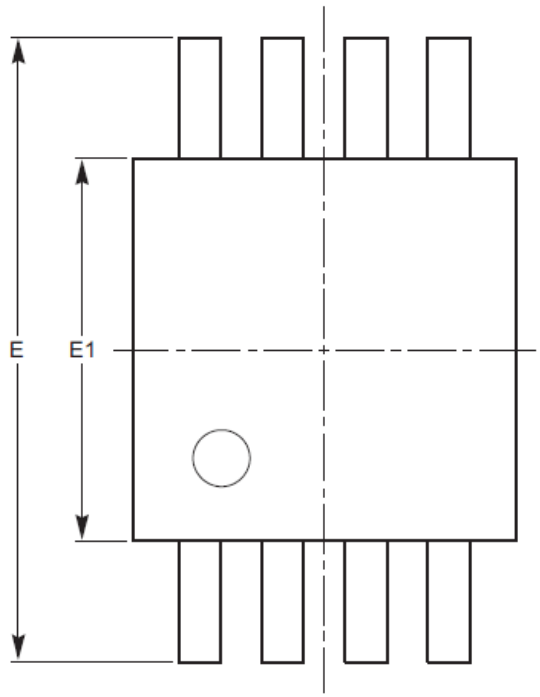
Packaging Information

SOP-8



SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	4.90		0.193	
E	5.80	6.20	0.228	0.244
E1	3.90		0.153	
L	0.40	1.27	0.016	0.050
b	0.31	0.51	0.012	0.020
e	1.27		0.050	

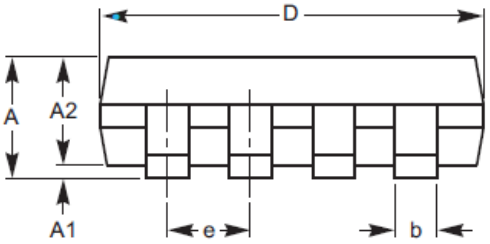
MSOP8



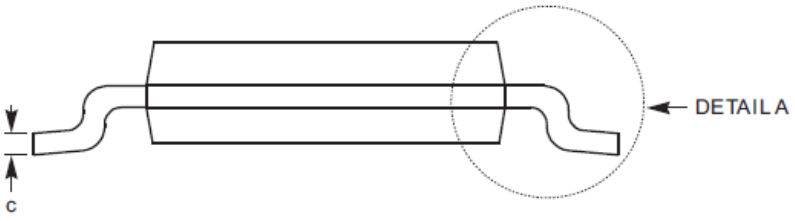
TOP VIEW

unit:mm

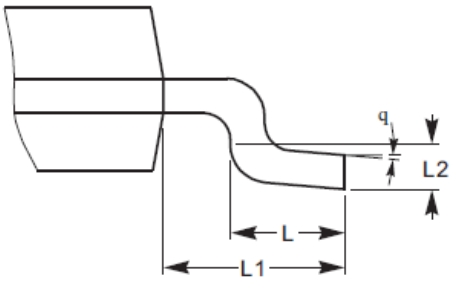
SYMBOL	MIN	NOM	MAX
A			1.10
A1	0.05	0.10	0.15
A2	0.75	0.85	0.95
b	0.22		0.38
c	0.13		0.23
D	2.90	3.00	3.10
E	4.80	4.90	5.00
E1	2.90	3.00	3.10
e		0.65 BSC	
L	0.40	0.60	0.80
L1		0.95 REF	
L2		0.25 BSC	
q	0°		6°



SIDE VIEW



END VIEW



DETAIL A