Dual 50MHz to 1000MHz High-Linearity, Serial/Parallel-Controlled Analog/Digital VGA

General Description

The MAX2062 high-linearity, dual analog/digital variable-gain amplifier (VGA) operates in the 50MHz to 1000MHz frequency range with two independent attenuators in each signal path. Each digital attenuator is controlled as a slave peripheral using either the SPI-compatible interface, or a 5-bit parallel bus with 31dB total adjustment range in 1dB steps. An added feature allows rapid-fire gain selection among each of the four steps, preprogrammed by the user through the SPI-compatible interface. A separate 2-pin control lets the user quickly access any one of four customized attenuation states without reprogramming the SPI bus. Each analog attenuator is controlled using an external voltage or through the SPI-compatible interface using an on-chip 8-bit DAC.

Since each of the stages has its own external RF input and RF output, this component can be configured to either optimize noise figure (NF) (amplifier configured first), OIP3 (amplifier last), or a compromise of NF and OIP3. The device's performance features include 24dB amplifier gain (amplifier only), 7.3dB NF at maximum gain (includes attenuator insertion losses), and a high OIP3 level of +41dBm. Each of these features makes the device an ideal VGA for multipath receiver and transmitter applications.

In addition, the device operates from a single +5V supply with full performance or a +3.3V supply for an enhanced power-savings mode with lower performance. The device is available in a compact 48-pin TQFN package (7mm x 7mm) with an exposed pad. Electrical performance is guaranteed over the extended temperature range, from T_C = -40°C to +85°C.

Applications

IF and RF Gain Stages

Temperature-Compensation Circuits

GSM/EDGE Base Stations

WCDMA, TD-SCDMA, and cdma2000® Base Stations

WiMAX®, LTE, and TD-LTE Base Stations and Customer-Premise Equipment

Fixed Broadband Wireless Access

Wireless Local Loop

Features

- ♦ **Independently Controlled Dual Paths**
- ♦ **50MHz to 1000MHz RF Frequency Range**
- ♦ **Pin-Compatible Family Includes**
  - **MAX2063 (Digital-Only VGA)**
  - **MAX2064 (Analog-Only VGA)**
- ♦ **19.4dB (typ) Maximum Gain**
- ♦ **0.34dB Gain Flatness Over 100MHz Bandwidth**
- ♦ **64dB Gain Range (33dB Analog Plus 31dB Digital)**
- ♦ **56dB Path Isolation (at 200MHz)**
- ♦ **Built-In 8-Bit DACs for Analog Attenuation Control**
- ♦ **Supports Four Rapid-Fire Preprogrammed Attenuator States**
  - **Quickly Access Any One of Four Customized Attenuator States**
  - **Ideal for Fast-Attack, High-Level Blocker Protection**
  - **Protects ADC Overdrive Condition**
- ♦ **Excellent Linearity (Configured with Amp Last at 200MHz)**
  - **+41dBm OIP3**
  - **+56dBm OIP2**
  - **+19dBm Output 1dB Compression Point**
- ♦ **7.3dB Typical Noise Figure (at 200MHz)**
- ♦ **Fast, 25ns Digital Switching**
- ♦ **Very Low Digital VGA Amplitude Overshoot/ Undershoot**
- ♦ **Single +5V Supply (or +3.3V Operation)**
- ♦ **Amplifier Power-Down Mode for TDD Applications**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX2062ETM+	-40°C to +85°C	48 TQFN-EP*
MAX2062ETM+T	-40°C to +85°C	48 TQFN-EP*

+Denotes lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
T = Tape and reel.

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ABSOLUTE MAXIMUM RATINGS

$V_{CC\_AMP\_1}$, $V_{CC\_AMP\_2}$, V_{CC_RG} to GND ....-0.3V to +5.5V
STA_A_1, STA_A_2, STA_B_1, STA_B_2,
PD_1, PD_2, AMPSET to GND ....-0.3V to +3.6V
A_VCTL_1, A_VCTL_2 to GND............................-0.3V to +3.6V
DAT, $\overline{CS}$, CLK, AA_SP, DA_SP to GND...............-0.3V to +3.6V
D0_1, D1_1, D2_1, D3_1, D4_1, D0_2, D1_2,
D2_2, D3_2, D4_2 to GND ....-0.3V to +3.6V
AMP_IN_1, AMP_IN_2 to GND..........................+0.95V to +1.2V
AMP_OUT_1, AMP_OUT_2 to GND ....-0.3V to +5.5V
D_ATT_IN_1, D_ATT_IN_2, D_ATT_OUT_1,
D_ATT_OUT_2 to GND..0V to +3.6V
A_ATT_IN_1, A_ATT_IN_2, A_ATT_OUT_1,
A_ATT_OUT_2 to GND..0V to +3.6V
REG_OUT to GND...-0.3V to +3.6V
RF Input Power (D_ATT_IN_1, D_ATT_IN_2) .... +20dBm
RF Input Power (A_ATT_IN_1, A_ATT_IN_2) .... +20dBm
RF Input Power (AMP_IN_1, AMP_IN_2)...................... +18dBm
θ_{JC} (Notes 1, 2)... +12.3°C/W
θ_{JA} (Notes 2, 3)... +38°C/W
Continuous Power Dissipation (Note 1) 5.3W
Operating Case Temperature Range (Note 4) .. -40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range........................... -65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

Note 1: Based on junction temperature $T_J = T_C + (\theta_{JC} \times V_{CC} \times I_{CC})$. This formula can be used when the temperature of the exposed pad is known while the device is soldered down to a PCB. See the *Applications Information* section for details. The junction temperature must not exceed +150°C.

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to .

Note 3: Junction temperature $T_J = T_A + (\theta_{JA} \times V_{CC} \times I_{CC})$. This formula can be used when the ambient temperature of the PCB is known. The junction temperature must not exceed +150°C.

Note 4: T_C is the temperature on the exposed pad of the package. T_A is the ambient temperature of the device and PCB.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5.0V SUPPLY DC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, $V_{CC} = V_{CC\_AMP\_1} = V_{CC\_AMP\_2} = V_{CC\_RG}$ = 4.75V to 5.25V, AMPSET = 0, PD_1 = PD_2 = 0, T_C = -40°C to +85°C. Typical values are at $V_{CC\_}$ = 5.0V and T_C = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		4.75	5	5.25	V
Supply Current	I_{DC}			148	210	mA
Power-Down Current	I_{DCPD}	PD_1 = PD_2 = 1, V_{IH} = 3.3V		5.3	8	mA
Logic-Low Input Voltage	V_{IL}				0.5	V
Logic-High Input Voltage	V_{IH}		1.7		3.465	V
Input Logic Current	I_{IH}, I_{IL}		-1		+1	µA

3.3V SUPPLY DC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, $V_{CC} = V_{CC\_AMP\_1} = V_{CC\_AMP\_2} = V_{CC\_RG}$ = 3.135V to 3.465V, AMPSET = 1, PD_1 = PD_2 = 0, T_C = -40°C to +85°C. Typical values are at $V_{CC\_}$ = 3.3V and T_C = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		3.135	3.3	3.465	V
Supply Current	I_{DC}			87	145	mA
Power-Down Current	I_{DCPD}	PD_1 = PD_2 = 1, V_{IH} = 3.3V		4.5	8	mA
Logic-Low Input Voltage	V_{IL}			0.5		V
Logic-High Input Voltage	V_{IH}			1.7		V

RECOMMENDED AC OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RF Frequency	f_{RF}	(Note 5)	50		1000	MHz

5.0V SUPPLY AC ELECTRICAL CHARACTERISTICS (Each Path, Unless Otherwise Noted)

(*Typical Application Circuit*, V_{CC} = $V_{CC\_AMP\_1}$ = $V_{CC\_AMP\_2}$ = V_{CC_RG} = 4.75V to 5.25V, attenuators are set for maximum gain, RF ports are driven from 50Ω sources, AMPSET = 0, PD_1 = PD_2 = 0, 100MHz ≤ f_{RF} ≤ 500MHz, T_C = -40°C to +85°C. Typical values are at maximum gain setting, $V_{CC\_}$ = 5.0V, P_{IN} = -20dBm, f_{RF} = 350MHz, and T_C = +25°C, unless otherwise noted.) (Note 6)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Small-Signal Gain	G	f_{RF} = 50MHz		20.3		dB
		f_{RF} = 100MHz		19.9		
		f_{RF} = 200MHz		19.4		
		f_{RF} = 350MHz, T_C = +25°C	17.0	18.9	21.0	
		f_{RF} = 450MHz		18.6		
		f_{RF} = 750MHz		17.8		
		f_{RF} = 900MHz		16.5		
Gain vs. Temperature				-0.01		dB/°C
Gain Flatness vs. Frequency		From 100MHz to 200MHz		0.5		dB
		Any 100MHz frequency band from 200MHz to 500MHz		0.34		
Noise Figure	NF	f_{RF} = 50MHz		6.4		dB
		f_{RF} = 100MHz		6.8		
		f_{RF} = 200MHz		7.3		
		f_{RF} = 350MHz		7.6		
		f_{RF} = 450MHz		7.8		
		f_{RF} = 750MHz		8.7		
		f_{RF} = 900MHz		9.0		
Total Attenuation Range		Analog and digital combined		64.1		dB
Output Second-Order Intercept Point	OIP2	P_{OUT} = 0dBm/tone, Δf = 1MHz, $f_1 + f_2$		52.1		dBm
Path Isolation		RF input 1 amplified power measured at RF output 2 relative to RF output 1, all unused ports terminated to 50Ω		48.6		dB
		RF input 2 amplified signal measured at RF output 1 relative to RF output 2, all unused ports terminated to 50Ω		47.7		
Output Third-Order Intercept Point	OIP3	P_{OUT} = 0dBm/tone, Δf = 1MHz, f_{RF} = 50MHz		47.5		dBm
		P_{OUT} = 0dBm/tone, Δf = 1MHz, f_{RF} = 100MHz		43.4		
		P_{OUT} = 0dBm/tone, Δf = 1MHz, f_{RF} = 200MHz		41.3		
		P_{OUT} = 0dBm/tone, Δf = 1MHz, f_{RF} = 350MHz		37.4		
		P_{OUT} = 0dBm/tone, Δf = 1MHz, f_{RF} = 450MHz		35.1		
		P_{OUT} = 0dBm/tone, Δf = 1MHz, f_{RF} = 750MHz		28.8		
		P_{OUT} = 0dBm/tone, Δf = 1MHz, f_{RF} = 900MHz		25.8		
Output -1dB Compression Point	P_{1dB}	f_{RF} = 350MHz, T_C = +25°C (Note 7)	17	18.8		dBm

Dual 50MHz to 1000MHz High-Linearity, Serial/Parallel-Controlled Analog/Digital VGA

5.0V SUPPLY AC ELECTRICAL CHARACTERISTICS (Each Path, Unless Otherwise Noted) (continued)

(*Typical Application Circuit*, V_{CC} = $V_{CC\_AMP\_1}$ = $V_{CC\_AMP\_2}$ = V_{CC_RG} = 4.75V to 5.25V, attenuators are set for maximum gain, RF ports are driven from 50Ω sources, AMPSET = 0, PD_1 = PD_2 = 0, 100MHz ≤ f_{RF} ≤ 500MHz, T_C = -40°C to +85°C. Typical values are at maximum gain setting, $V_{CC\_}$ = 5.0V, P_{IN} = -20dBm, f_{RF} = 350MHz, and T_C = +25°C, unless otherwise noted.) (Note 6)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Second Harmonic		P_{OUT} = +3dBm			-55.0		dBc
Third Harmonic		P_{OUT} = +3dBm			-72.7		dBc
Group Delay		Includes EV kit PCB delays			1.03		ns
Amplifier Power-Down Time		PD_1 or PD_2 from 0 to 1, amplifier DC supply current settles to within 0.1mA			0.5		µs
Amplifier Power-Up Time		PD_1 or PD_2 from 1 to 0, amplifier DC supply current settles to within 1%			0.5		µs
Input Return Loss	RL_{IN}	50Ω source			16.1		dB
Output Return Loss	RL_{OUT}	50Ω load			30.8		dB
DIGITAL ATTENUATOR (Each Path, Unless Otherwise Noted)							
Insertion Loss					3.0		dB
Input Second-Order Intercept Point		P_{IN1} = 0dBm, P_{IN2} = 0dBm (minimum attenuation), Δf = 1MHz, $f_1 + f_2$			53.6		dBm
Input Third-Order Intercept Point		P_{IN1} = 0dBm, P_{IN2} = 0dBm (minimum attenuation), Δf = 1MHz			41.5		dBm
Attenuation Range		f_{RF} = 350MHz, T_C = +25°C, V_{CC} = 5.0V		29.5	30.9		dB
Step Size					1		dB
Relative Attenuation Accuracy					0.13		dB
Absolute Attenuation Accuracy					0.14		dB
Insertion Phase Step		f_{RF} = 170MHz	0dB to 16dB		0		Degrees
			0dB to 24dB		1.1		
			0dB to 31dB		1.2		
Amplitude Overshoot/Undershoot		Between any two states	Elapsed time = 15ns		1.0		dB
			Elapsed time = 40ns		0.05		
Switching Speed		RF settled to within ±0.1dB	31dB to 0dB		25		ns
			0dB to 31dB		21		
Input Return Loss		50Ω source			22.0		dB
Output Return Loss		50Ω load			21.9		dB
ANALOG ATTENUATOR (Each Path, Unless Otherwise Noted)							
Insertion Loss					2.2		dB
Input Second-Order Intercept Point		P_{IN1} = 0dBm, P_{IN2} = 0dBm (minimum attenuation), Δf = 1MHz, $f_1 + f_2$			61.9		dBm
Input Third-Order Intercept Point		P_{IN1} = 0dBm, P_{IN2} = 0dBm (minimum attenuation), Δf = 1MHz			37.0		dBm

5.0V SUPPLY AC ELECTRICAL CHARACTERISTICS (Each Path, Unless Otherwise Noted) (continued)

(*Typical Application Circuit*, V_{CC} = $V_{CC\_AMP\_1}$ = $V_{CC\_AMP\_2}$ = V_{CC_RG} = 4.75V to 5.25V, attenuators are set for maximum gain, RF ports are driven from 50Ω sources, AMPSET = 0, PD_1 = PD_2 = 0, 100MHz ≤ f_{RF} ≤ 500MHz, T_C = -40°C to +85°C. Typical values are at maximum gain setting, $V_{CC\_}$ = 5.0V, P_{IN} = -20dBm, f_{RF} = 350MHz, and T_C = +25°C, unless otherwise noted.) (Note 6)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Attenuation Range		f_{RF} = 350MHz, T_C = +25°C, V_{CC} = 5.0V		29.5	33.2		dB
Gain Control Slope		Analog control input			-13.3		dB/V
Maximum Gain Control Slope		Over analog control input range			-35.2		dB/V
Insertion Phase Change		Over analog control input range			17.6		Deg
Attenuator Response Time		RF settled to within ±0.5dB	AA_SP = 0, $V_{A\_VCTL\_\_}$ from 2.75V to 0.25V		500		ns
			AA_SP = 1, DAC code from 11111111 to 00000000, from $\overline{CS}$ rising edge		500		
			AA_SP = 0, $V_{A\_VCTL\_\_}$ from 0.25V to 2.75V		500		
			AA_SP = 1, DAC code from 00000000 to 11111111, from $\overline{CS}$ rising edge		500		
Group Delay vs. Control Voltage		Over analog control input from 0.25V to 2.75V			-0.34		ns
Analog Control Input Range				0.25		2.75	V
Analog Control Input Impedance					19.2		kΩ
Input Return Loss		50Ω source			16.1		dB
Output Return Loss		50Ω load			16.8		dB
D/A CONVERTER							
Number of Bits					8		Bits
Output Voltage		DAC code = 00000000				0.35	V
		DAC code = 11111111		2.7			
SERIAL PERIPHERAL INTERFACE (SPI)							
Maximum Clock Speed					20		MHz
Data-to-Clock Setup Time	t_{CS}				2		ns
Data-to-Clock Hold Time	t_{CH}				2.5		ns
Clock-to-$\overline{CS}$ Setup Time	t_{ES}				3		ns
$\overline{CS}$ Positive Pulse Width	t_{EW}				7		ns
$\overline{CS}$ Setup Time	t_{EWS}				3.5		ns
Clock Pulse Width	t_{CW}				5		ns

3.3V SUPPLY AC ELECTRICAL CHARACTERISTICS (Each Path, Unless Otherwise Noted)

(*Typical Application Circuit*, $V_{CC} = V_{CC\_AMP\_1} = V_{CC\_AMP\_2} = V_{CC\_RG}$ = 3.135V to 3.465V, attenuators are set for maximum gain, RF ports are driven from 50Ω sources, AMPSET = 1, PD_1 = PD_2 = 0, 100MHz ≤ f_{RF} ≤ 500MHz, T_C = -40°C to +85°C. Typical values are at maximum gain setting, $V_{CC\_}$ = 3.3V, P_{IN} = -20dBm, f_{RF} = 350MHz, and T_C = +25°C, unless otherwise noted.) (Note 6)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Small-Signal Gain				18.8		dB
Output Third-Order Intercept Point	OIP3	P_{OUT} = 0dBm/tone		29.4		dBm
Noise Figure				7.8		dB
Total Attenuation Range				64.1		dB
Path Isolation		RF input 1 amplified power measured at RF output 2 relative to RF output 1, all unused ports terminated to 50Ω		49.1		dB
		RF input 2 amplified signal measured at RF output 1 relative to RF output 2, all unused ports terminated to 50Ω		48.0		
Output -1dB Compression Point	P_{1dB}	(Note 7)		13.4		dBm

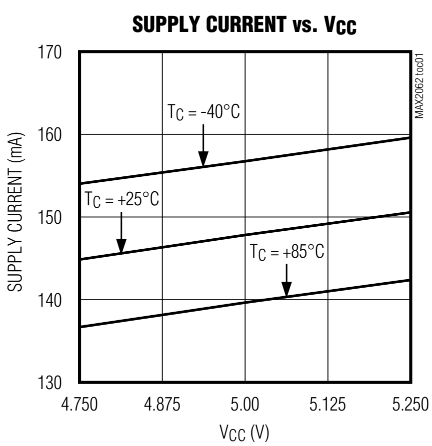
Note 5: Operation outside this range is possible, but with degraded performance of some parameters. See the *Typical Operating Characteristics* section.

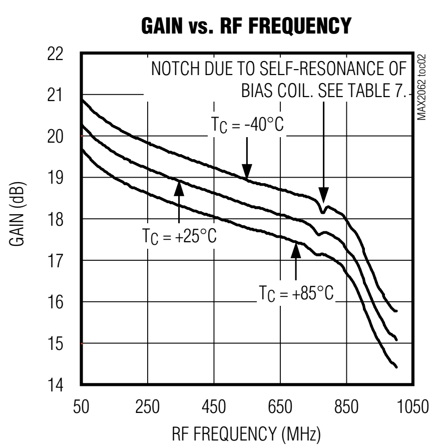
Note 6: All limits include external component losses. Output measurements are performed at the RF output port of the *Typical Application Circuit*.

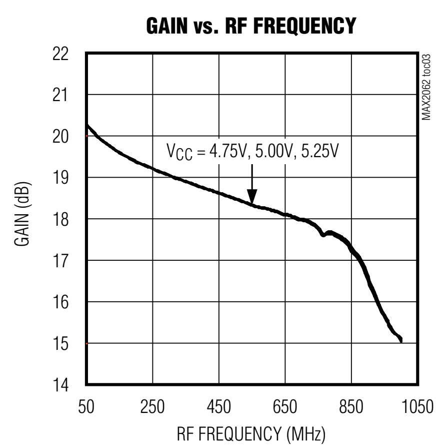
Note 7: It is advisable not to continuously operate the RF input 1 or RF input 2 above +15dBm.

Typical Operating Characteristics

(*Typical Application Circuit*, **$V_{CC} = V_{CC\_AMP\_1} = V_{CC\_AMP\_2} = V_{CC\_RG}$ = 5.0V**, attenuators are set for maximum gain, RF ports are driven from 50Ω sources, AMPSET = 0, PD_1 = PD_2 = 0, P_{IN} = -20dBm, f_{RF} = 350MHz, and T_C = +25°C, unless otherwise noted.)



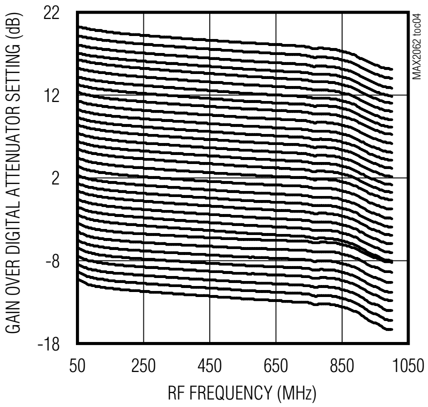




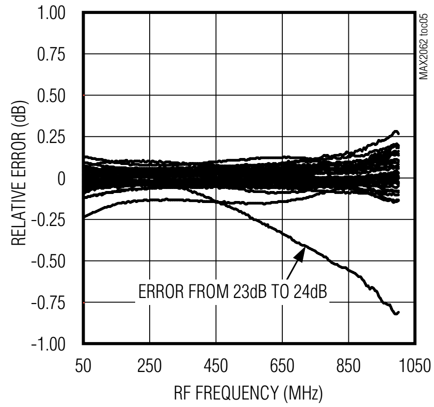
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, **V_{CC} = $V_{CC\_AMP\_1}$ = $V_{CC\_AMP\_2}$ = V_{CC_RG} = 5.0V**, attenuators are set for maximum gain, RF ports are driven from 50Ω sources, AMPSET = 0, PD_1 = PD_2 = 0, P_{IN} = -20dBm, f_{RF} = 350MHz, and T_C = +25°C, unless otherwise noted.)

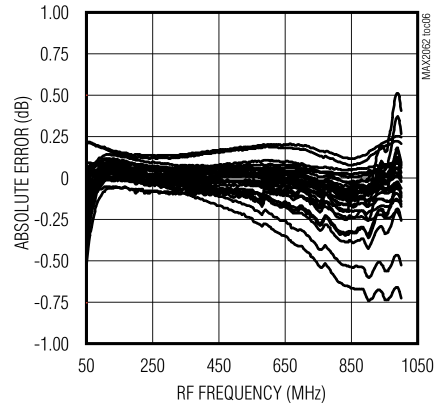
GAIN OVER DIGITAL ATTENUATOR SETTING vs. RF FREQUENCY



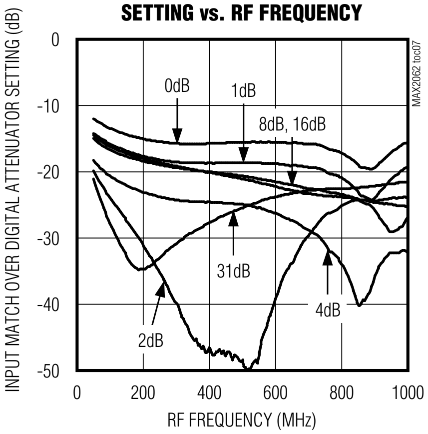
DIGITAL ATTENUATOR RELATIVE ERROR vs. RF FREQUENCY



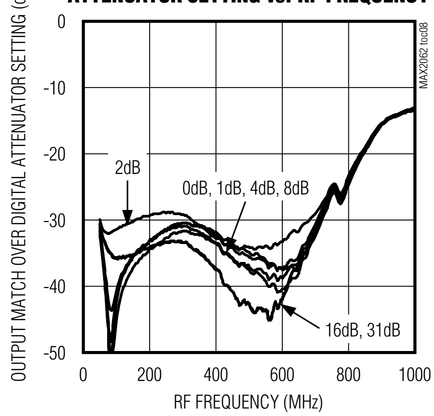
DIGITAL ATTENUATOR ABSOLUTE ERROR vs. RF FREQUENCY



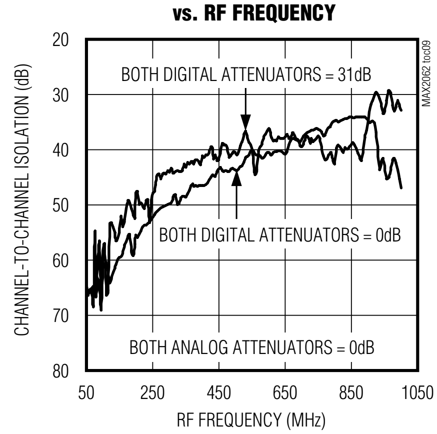
INPUT MATCH OVER DIGITAL ATTENUATOR SETTING vs. RF FREQUENCY



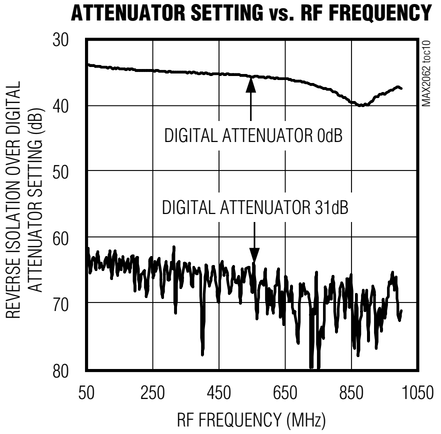
OUTPUT MATCH OVER DIGITAL ATTENUATOR SETTING vs. RF FREQUENCY



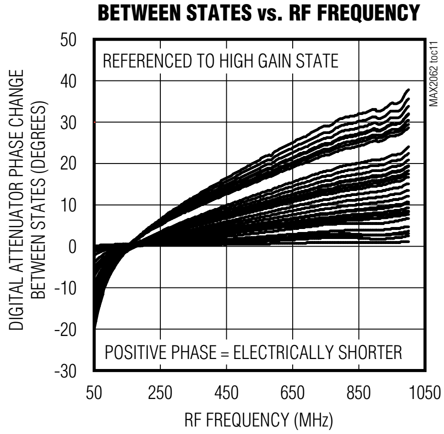
CHANNEL-TO-CHANNEL ISOLATION vs. RF FREQUENCY



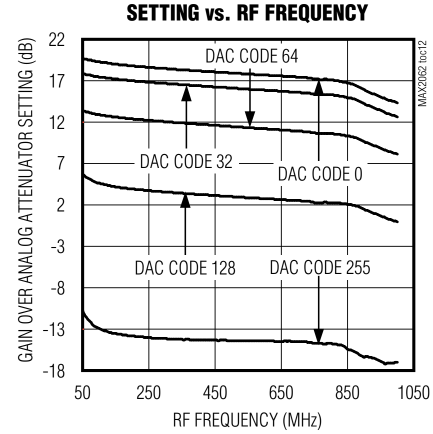
REVERSE ISOLATION OVER DIGITAL ATTENUATOR SETTING vs. RF FREQUENCY



DIGITAL ATTENUATOR PHASE CHANGE BETWEEN STATES vs. RF FREQUENCY



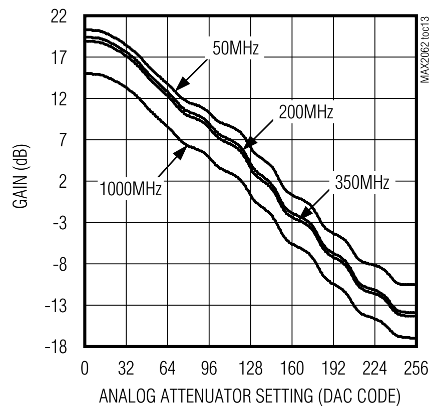
GAIN OVER ANALOG ATTENUATOR SETTING vs. RF FREQUENCY



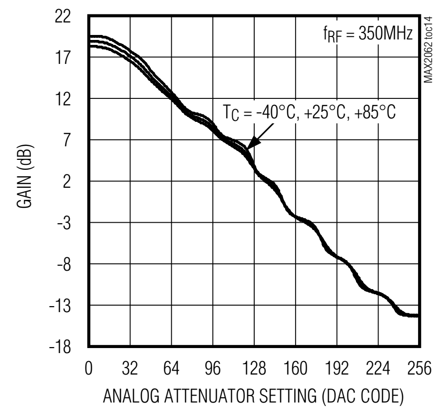
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, **V_{CC} = $V_{CC\_AMP\_1}$ = $V_{CC\_AMP\_2}$ = V_{CC_RG} = 5.0V**, attenuators are set for maximum gain, RF ports are driven from 50Ω sources, AMPSET = 0, PD_1 = PD_2 = 0, P_{IN} = -20dBm, f_{RF} = 350MHz, and T_C = +25°C, unless otherwise noted.)

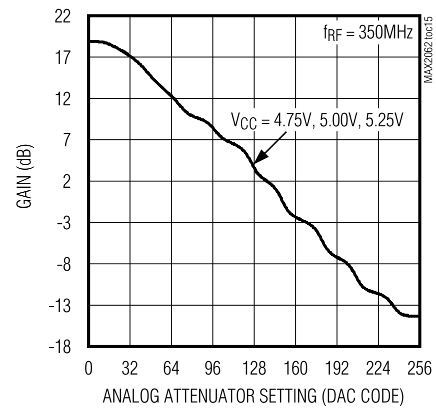
GAIN vs. ANALOG ATTENUATOR SETTING



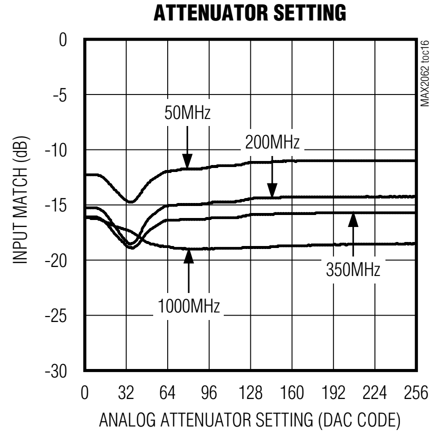
GAIN vs. ANALOG ATTENUATOR SETTING



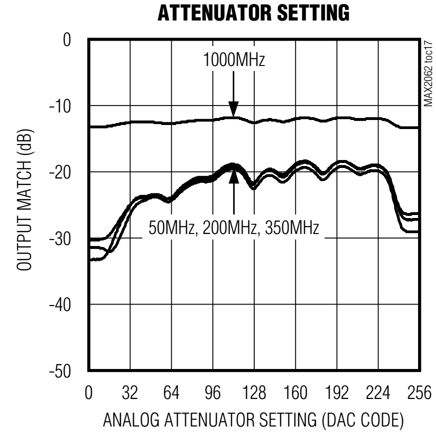
GAIN vs. ANALOG ATTENUATOR SETTING



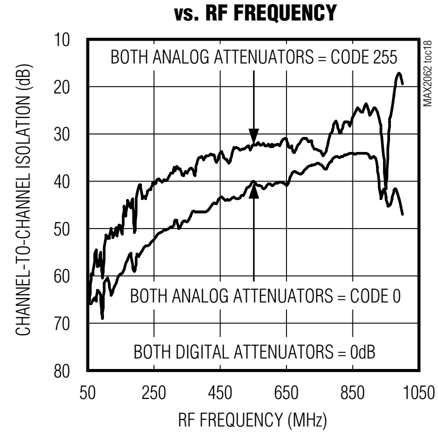
INPUT MATCH vs. ANALOG ATTENUATOR SETTING



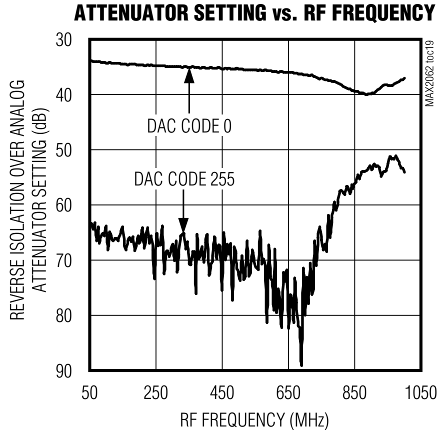
OUTPUT MATCH vs. ANALOG ATTENUATOR SETTING



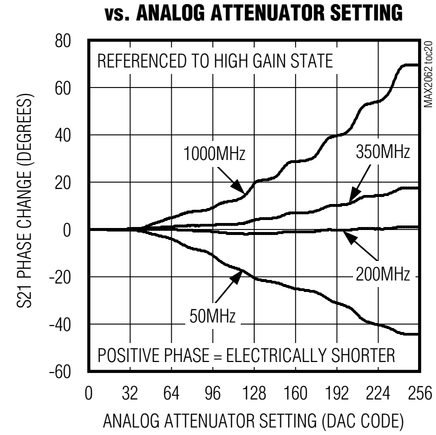
CHANNEL-TO-CHANNEL ISOLATION vs. RF FREQUENCY



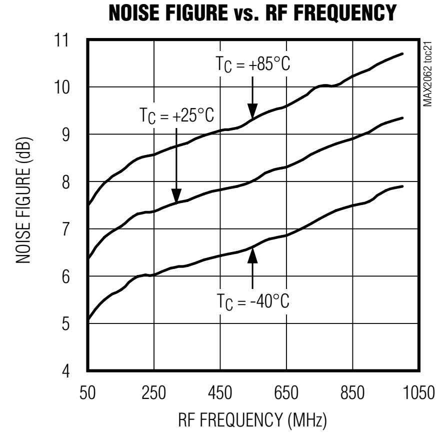
REVERSE ISOLATION OVER ANALOG ATTENUATOR SETTING vs. RF FREQUENCY



S21 PHASE CHANGE vs. ANALOG ATTENUATOR SETTING



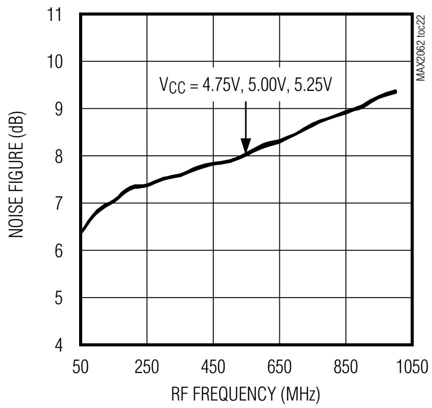
NOISE FIGURE vs. RF FREQUENCY



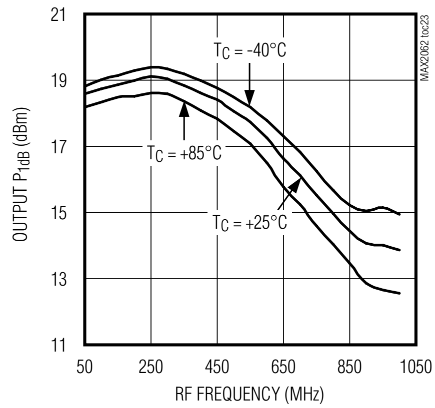
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, **V_{CC} = $V_{CC\_AMP\_1}$ = $V_{CC\_AMP\_2}$ = V_{CC_RG} = 5.0V**, attenuators are set for maximum gain, RF ports are driven from 50Ω sources, AMPSET = 0, PD_1 = PD_2 = 0, P_{IN} = -20dBm, f_{RF} = 350MHz, and T_C = +25°C, unless otherwise noted.)

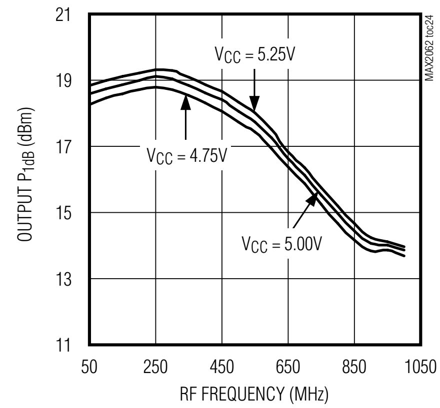
NOISE FIGURE vs. RF FREQUENCY



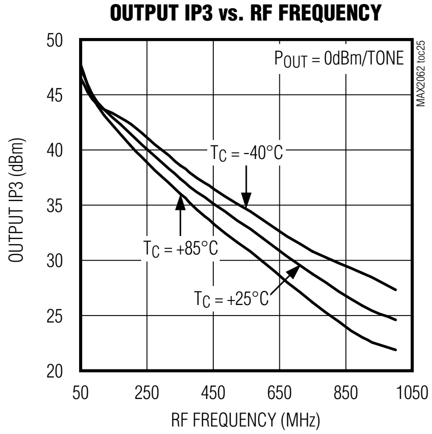
OUTPUT P1dB vs. RF FREQUENCY



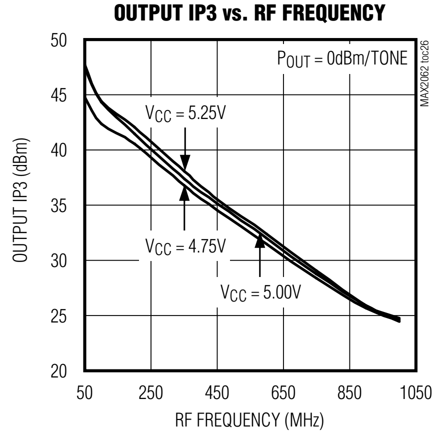
OUTPUT P1dB vs. RF FREQUENCY



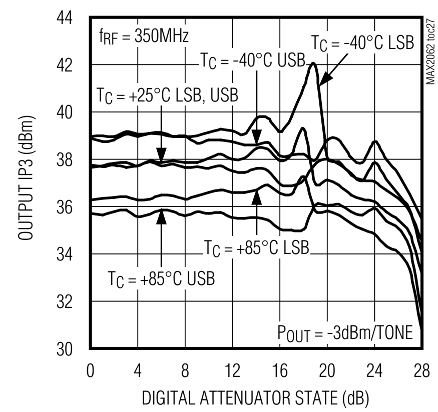
OUTPUT IP3 vs. RF FREQUENCY



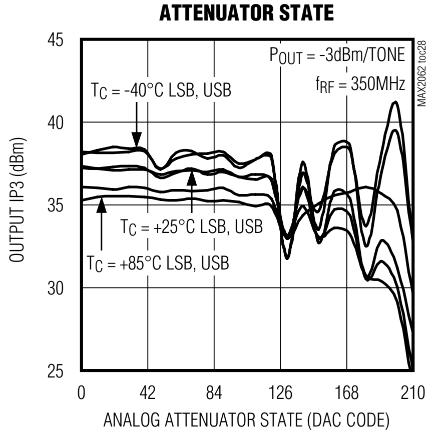
OUTPUT IP3 vs. RF FREQUENCY



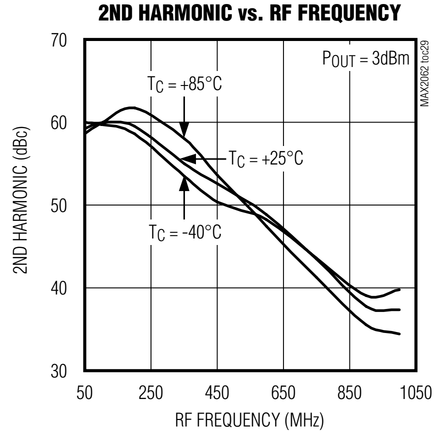
OUTPUT IP3 vs. DIGITAL ATTENUATOR STATE



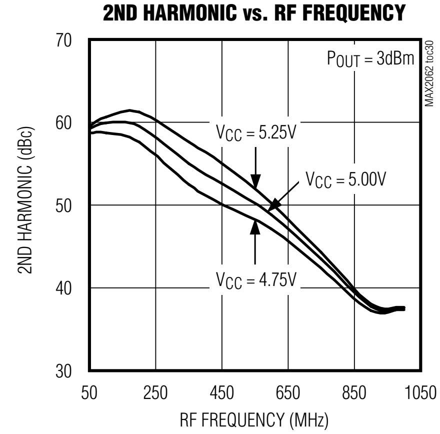
OUTPUT IP3 vs. ANALOG ATTENUATOR STATE



2ND HARMONIC vs. RF FREQUENCY



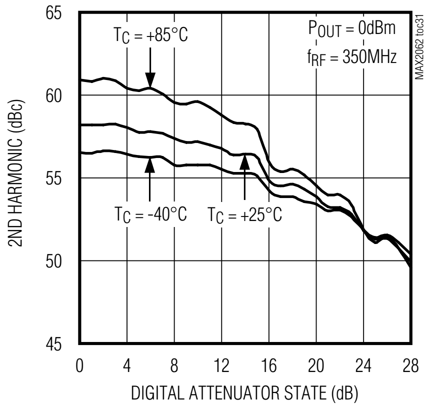
2ND HARMONIC vs. RF FREQUENCY



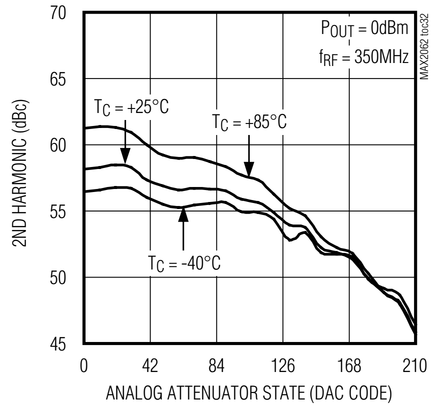
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, **$V_{CC} = V_{CC\_AMP\_1} = V_{CC\_AMP\_2} = V_{CC\_RG}$ = 5.0V**, attenuators are set for maximum gain, RF ports are driven from 50Ω sources, AMPSET = 0, PD_1 = PD_2 = 0, P_{IN} = -20dBm, f_{RF} = 350MHz, and T_C = +25°C, unless otherwise noted.)

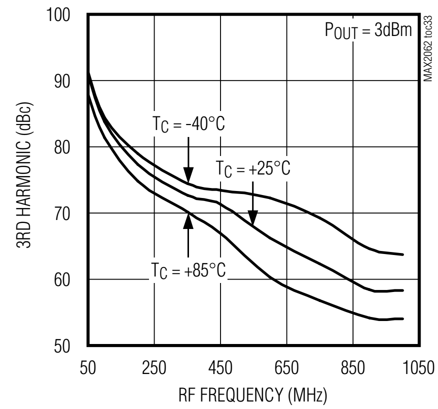
2ND HARMONIC vs. DIGITAL ATTENUATOR STATE



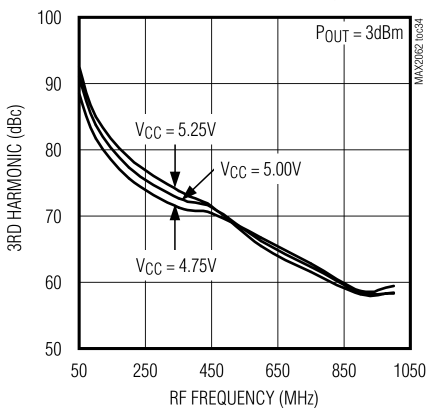
2ND HARMONIC vs. ANALOG ATTENUATOR STATE



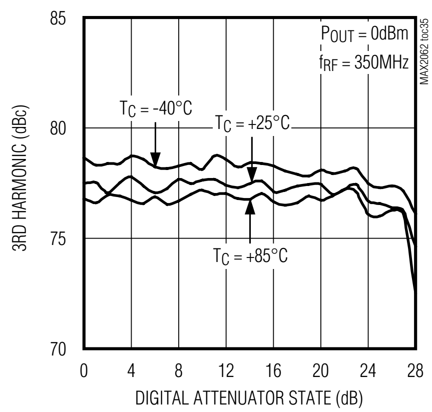
3RD HARMONIC vs. RF FREQUENCY



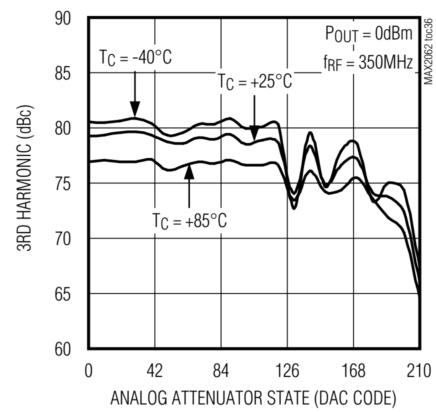
3RD HARMONIC vs. RF FREQUENCY



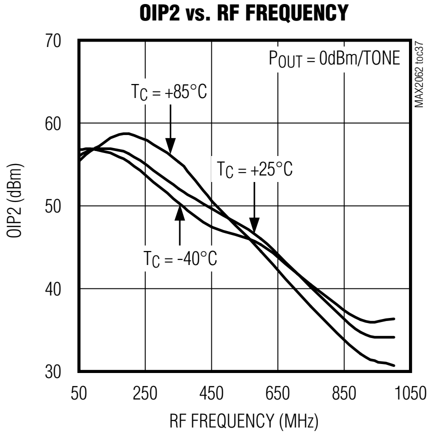
3RD HARMONIC vs. DIGITAL ATTENUATOR STATE



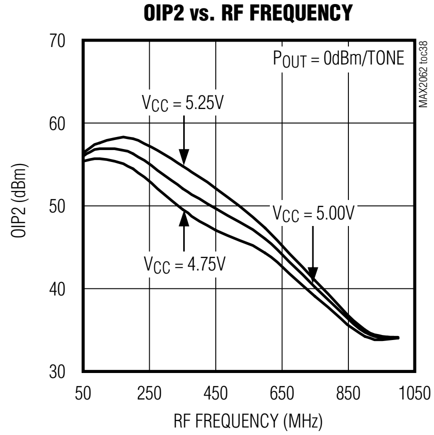
3RD HARMONIC vs. ANALOG ATTENUATOR STATE



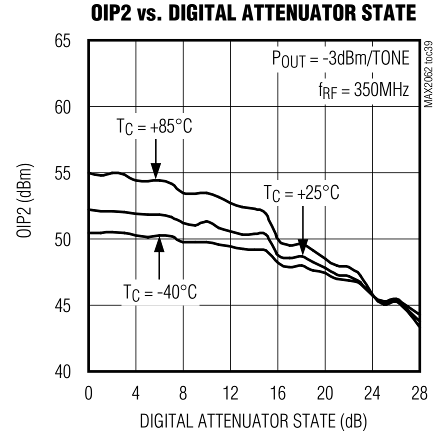
OIP2 vs. RF FREQUENCY



OIP2 vs. RF FREQUENCY



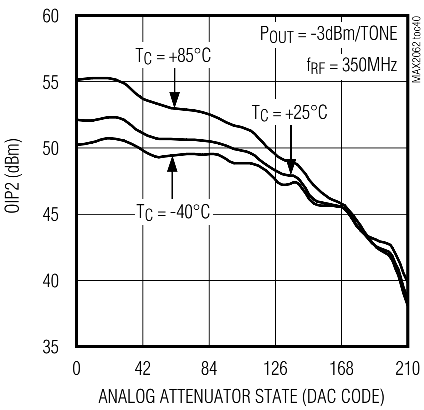
OIP2 vs. DIGITAL ATTENUATOR STATE



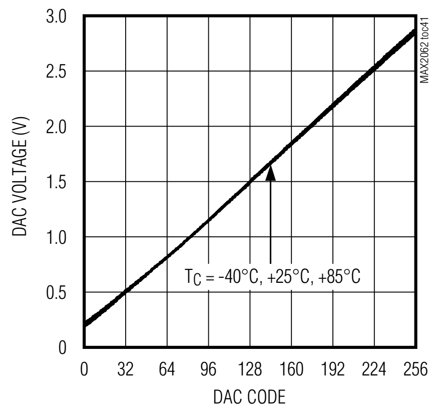
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, **V_{CC} = $V_{CC\_AMP\_1}$ = $V_{CC\_AMP\_2}$ = V_{CC_RG} = 5.0V**, attenuators are set for maximum gain, RF ports are driven from 50Ω sources, AMPSET = 0, PD_1 = PD_2 = 0, P_{IN} = -20dBm, f_{RF} = 350MHz, and T_C = +25°C, unless otherwise noted.)

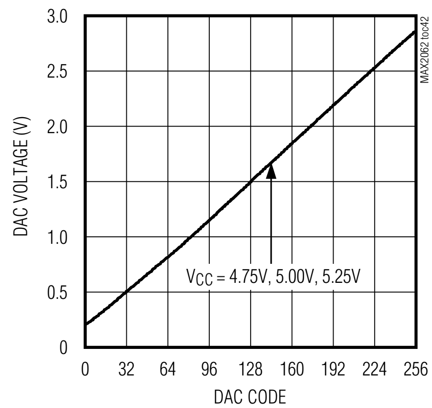
OIP2 vs. ANALOG ATTENUATOR STATE



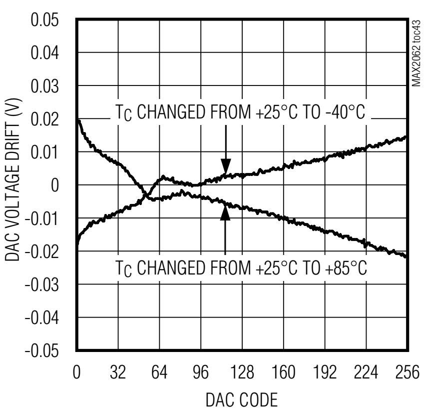
DAC VOLTAGE vs. DAC CODE



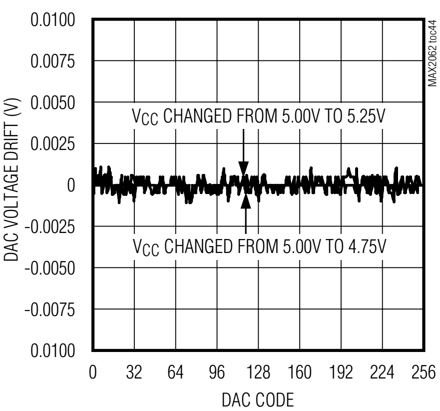
DAC VOLTAGE vs. DAC CODE



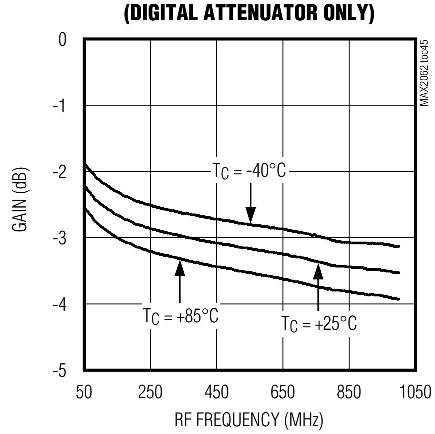
DAC VOLTAGE DRIFT vs. DAC CODE



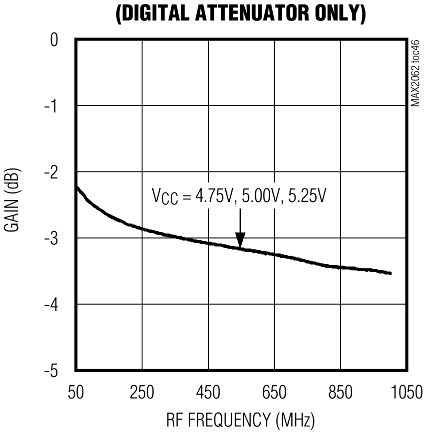
DAC VOLTAGE DRIFT vs. DAC CODE



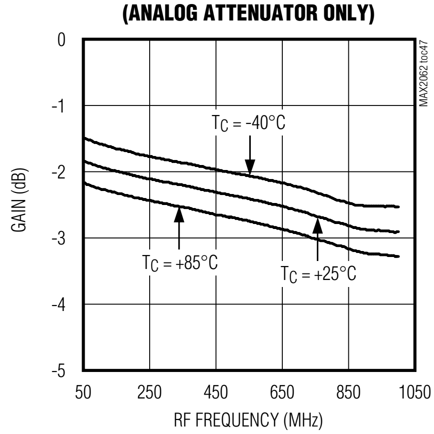
GAIN vs. RF FREQUENCY (DIGITAL ATTENUATOR ONLY)



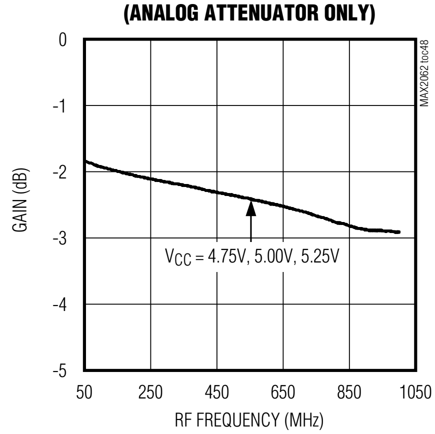
GAIN vs. RF FREQUENCY (DIGITAL ATTENUATOR ONLY)



GAIN vs. RF FREQUENCY (ANALOG ATTENUATOR ONLY)



GAIN vs. RF FREQUENCY (ANALOG ATTENUATOR ONLY)

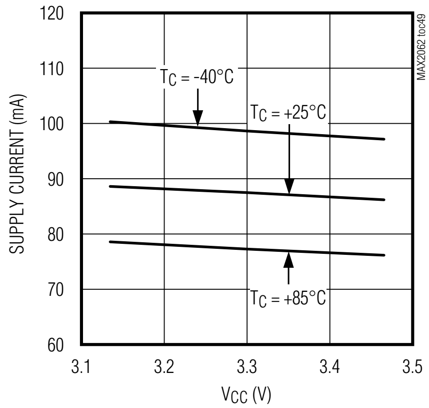


Dual 50MHz to 1000MHz High-Linearity, Serial/Parallel-Controlled Analog/Digital VGA

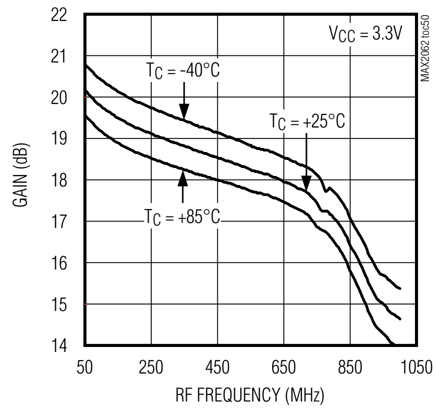
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, **$V_{CC} = V_{CC\_AMP\_1} = V_{CC\_AMP\_2} = V_{CC\_RG}$ = 3.3V**, attenuators are set for maximum gain, RF ports are driven from 50Ω sources, AMPSET = 1, PD_1 = PD_2 = 0, P_{IN} = -20dBm, f_{RF} = 350MHz, and T_C = +25°C, unless otherwise noted.)

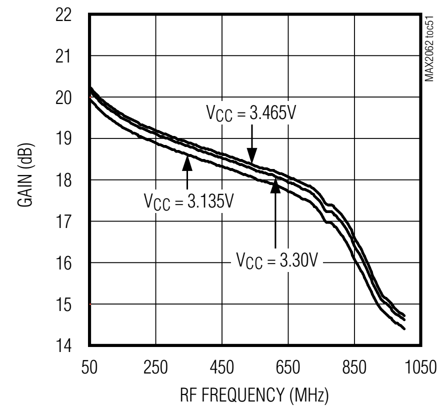
SUPPLY CURRENT vs. V_{CC}



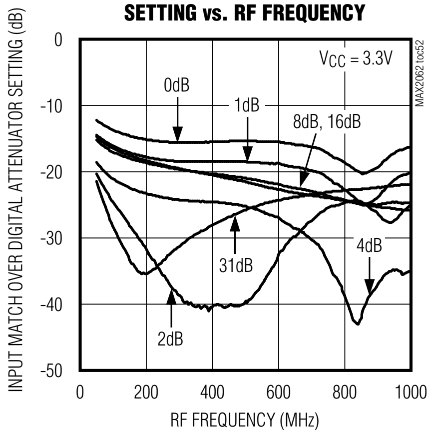
GAIN vs. RF FREQUENCY



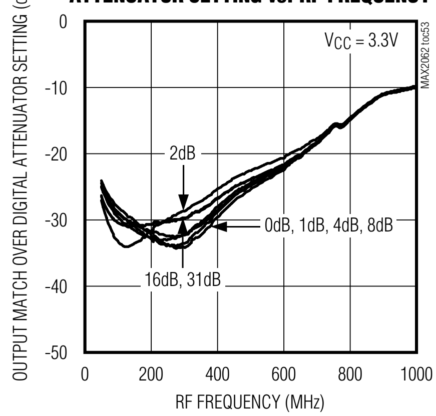
GAIN vs. RF FREQUENCY



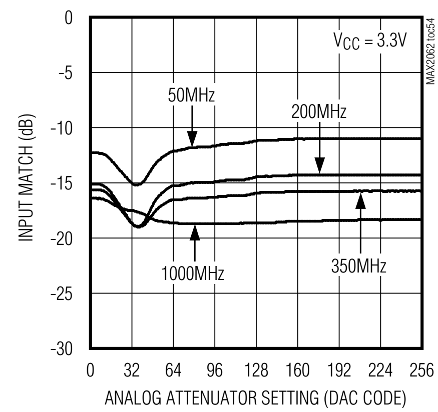
INPUT MATCH OVER DIGITAL ATTENUATOR SETTING vs. RF FREQUENCY



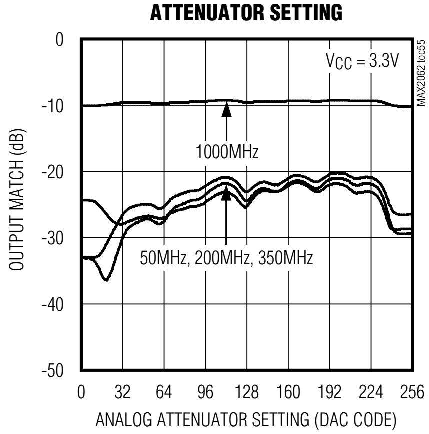
OUTPUT MATCH OVER DIGITAL ATTENUATOR SETTING vs. RF FREQUENCY



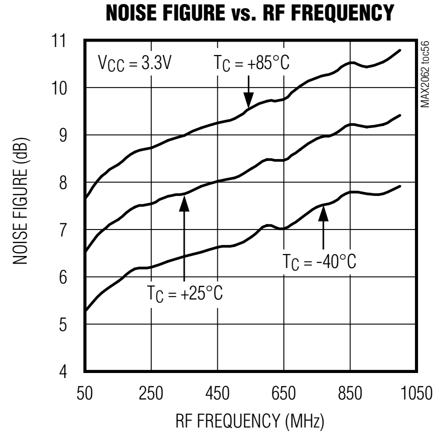
INPUT MATCH vs. ANALOG ATTENUATOR SETTING



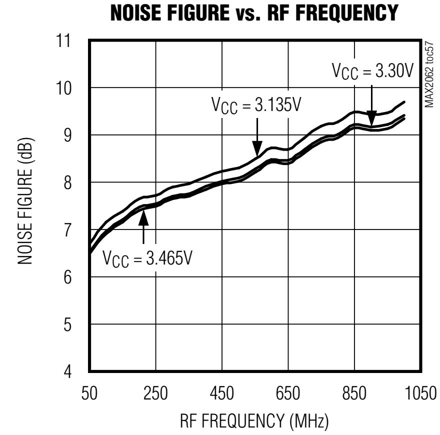
OUTPUT MATCH vs. ANALOG ATTENUATOR SETTING



NOISE FIGURE vs. RF FREQUENCY



NOISE FIGURE vs. RF FREQUENCY

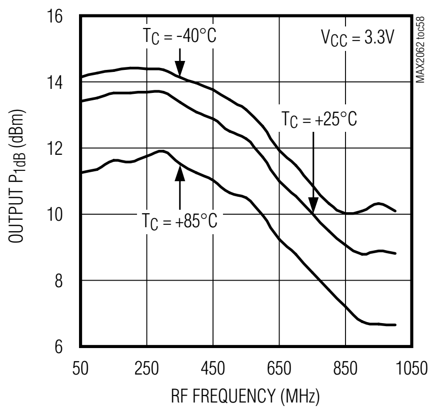


Dual 50MHz to 1000MHz High-Linearity, Serial/Parallel-Controlled Analog/Digital VGA

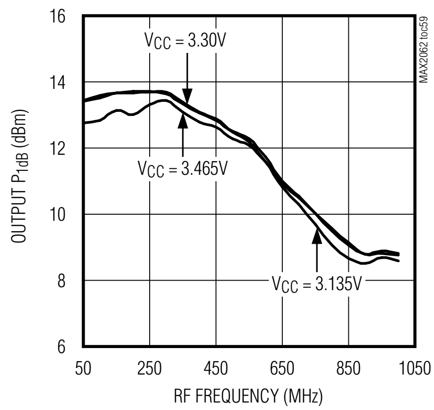
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, **V_{CC} = $V_{CC\_AMP\_1}$ = $V_{CC\_AMP\_2}$ = V_{CC_RG} = 3.3V**, attenuators are set for maximum gain, RF ports are driven from 50Ω sources, AMPSET = 1, PD_1 = PD_2 = 0, P_{IN} = -20dBm, f_{RF} = 350MHz, and T_C = +25°C, unless otherwise noted.)

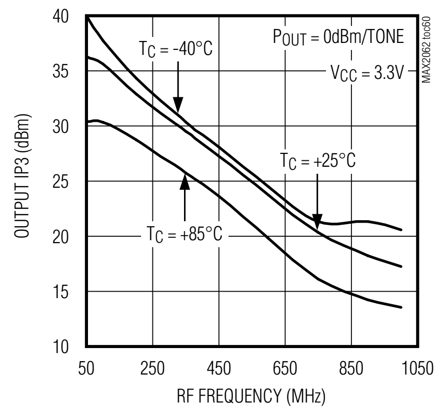
OUTPUT P_{1dB} vs. RF FREQUENCY



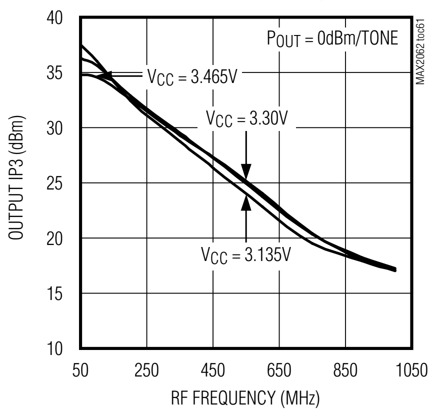
OUTPUT P_{1dB} vs. RF FREQUENCY



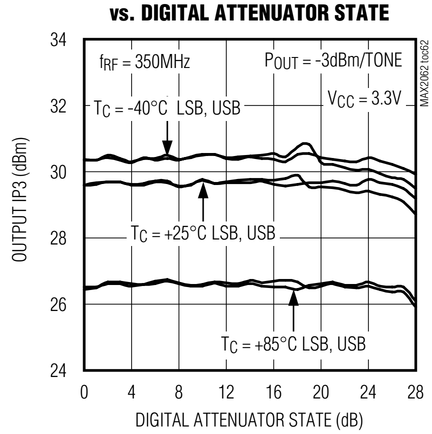
OUTPUT IP3 vs. RF FREQUENCY



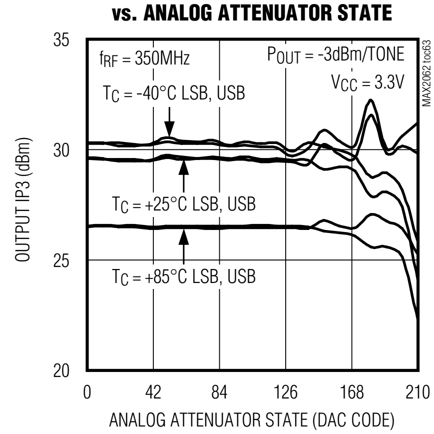
OUTPUT IP3 vs. RF FREQUENCY



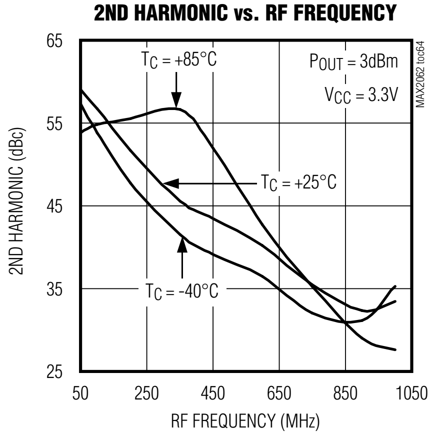
OUTPUT IP3 vs. DIGITAL ATTENUATOR STATE



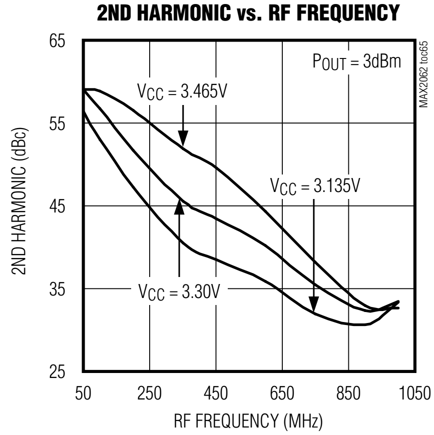
OUTPUT IP3 vs. ANALOG ATTENUATOR STATE



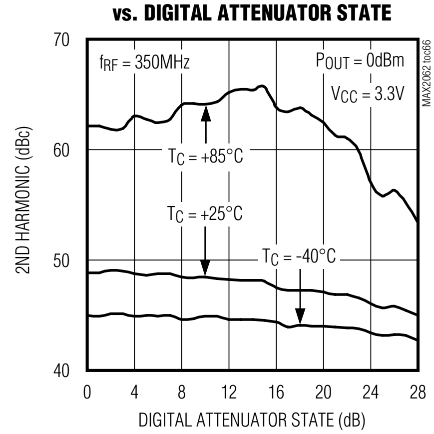
2ND HARMONIC vs. RF FREQUENCY



2ND HARMONIC vs. RF FREQUENCY



2ND HARMONIC vs. DIGITAL ATTENUATOR STATE



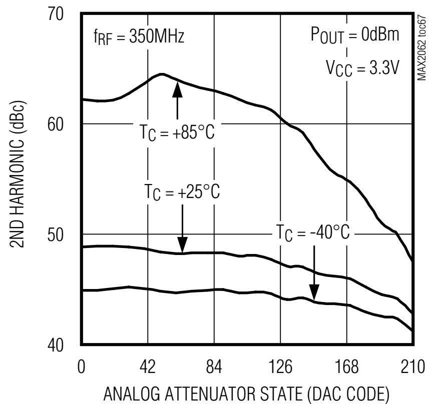
MAX2062

Dual 50MHz to 1000MHz High-Linearity, Serial/Parallel-Controlled Analog/Digital VGA

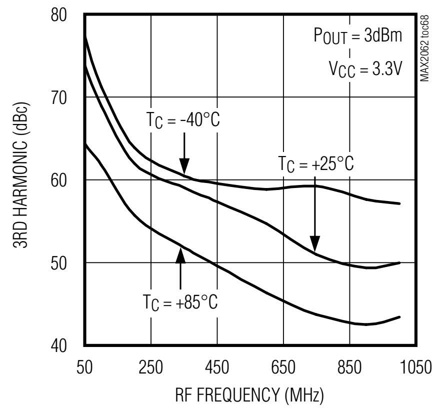
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, **V_{CC} = $V_{CC\_AMP\_1}$ = $V_{CC\_AMP\_2}$ = V_{CC_RG} = 3.3V**, attenuators are set for maximum gain, RF ports are driven from 50Ω sources, AMPSET = 1, PD_1 = PD_2 = 0, P_{IN} = -20dBm, f_{RF} = 350MHz, and T_C = +25°C, unless otherwise noted.)

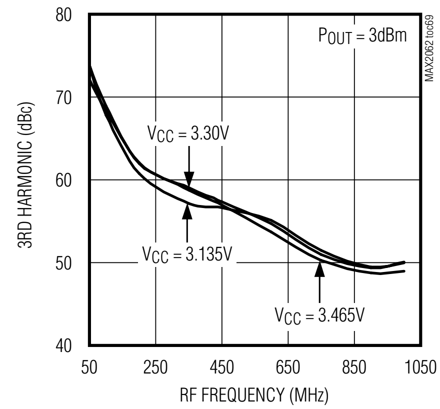
2ND HARMONIC vs. ANALOG ATTENUATOR STATE



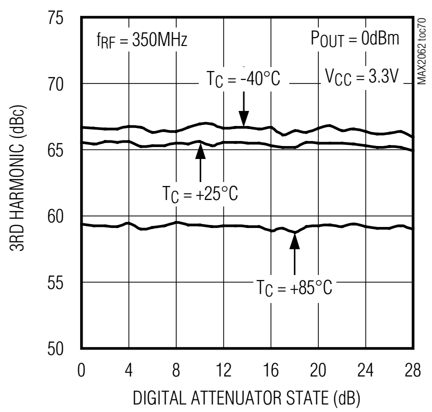
3RD HARMONIC vs. RF FREQUENCY



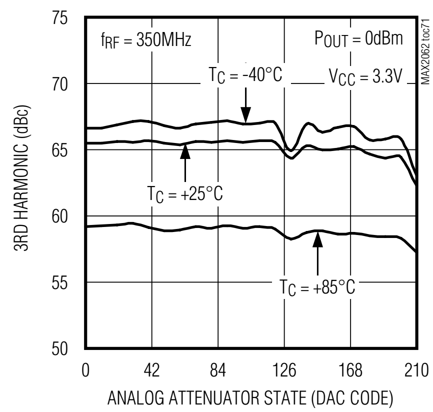
3RD HARMONIC vs. RF FREQUENCY



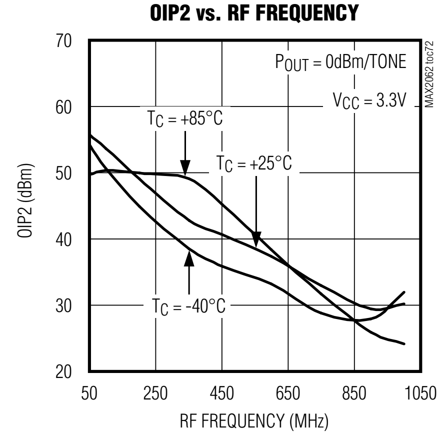
3RD HARMONIC vs. DIGITAL ATTENUATOR STATE



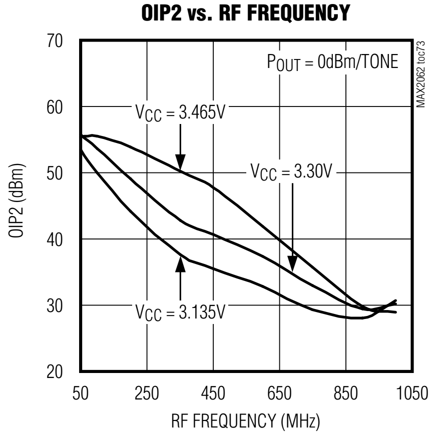
3RD HARMONIC vs. ANALOG ATTENUATOR STATE



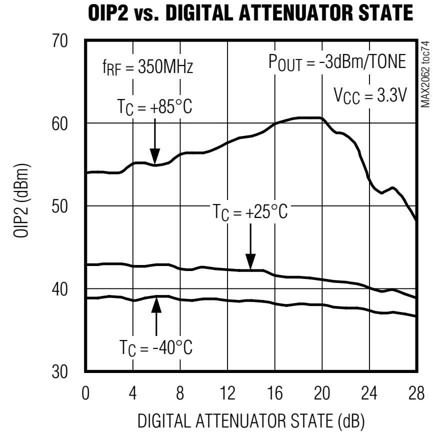
OIP2 vs. RF FREQUENCY



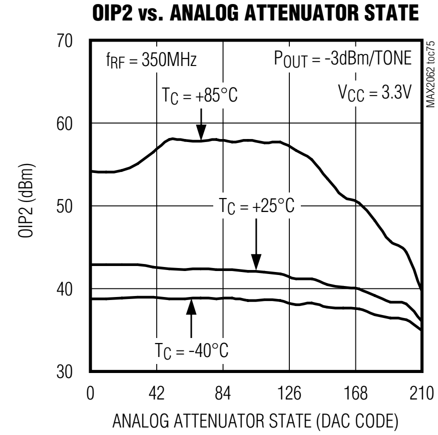
OIP2 vs. RF FREQUENCY



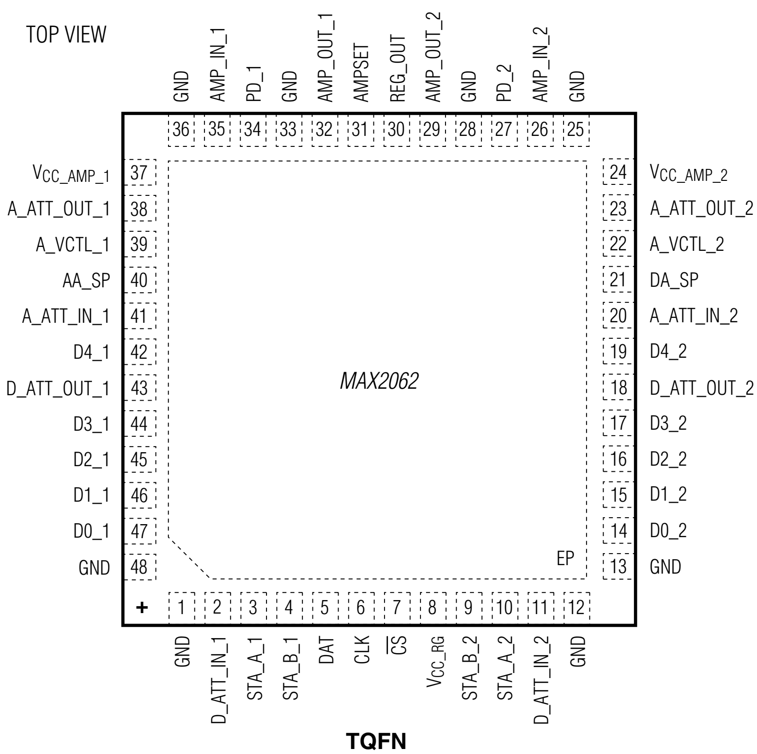
OIP2 vs. DIGITAL ATTENUATOR STATE



OIP2 vs. ANALOG ATTENUATOR STATE



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1, 12, 13, 25, 28, 33, 36, 48	GND	Ground
2	D_ATT_IN_1	5-Bit Digital Attenuator Input (50Ω), Path 1. Requires a DC-blocking capacitor.
3	STA_A_1	Digital Attenuator Preprogrammed Attenuation-State Logic Input, Path 1 **State A** / **State B** / **Digital Attenuator** Logic = 0 / Logic = 0 / Preprogrammed State 1 Logic = 1 / Logic = 0 / Preprogrammed State 2 Logic = 0 / Logic = 1 / Preprogrammed State 3 Logic = 1 / Logic = 1 / Preprogrammed State 4
4	STA_B_1	
5	DAT	SPI Data Digital Input
6	CLK	SPI Clock Digital Input
7	$\overline{CS}$	SPI Chip-Select Digital Input
8	V_{CC_RG}	Regulator Supply Input. Connect to a 3.3V or 5V external power supply. V_{CC_RG} powers all circuits except for the driver amplifiers. Bypass with a 10nF capacitor as close as possible to the pin.

Pin Description (continued)

PIN	NAME	FUNCTION
9	STA_B_2	Digital Attenuator Preprogrammed Attenuation-State Logic Input, Path 2 **State A** / **State B** / **Digital Attenuator** Logic = 0 / Logic = 0 / Preprogrammed State 1 Logic = 1 / Logic = 0 / Preprogrammed State 2 Logic = 0 / Logic = 1 / Preprogrammed State 3 Logic = 1 / Logic = 1 / Preprogrammed State 4
10	STA_A_2	
11	D_ATT_IN_2	5-Bit Digital Attenuator Input (50Ω), Path 2. Requires a DC-blocking capacitor.
14	D0_2	1dB Attenuator Logic Input, Path 2. Logic 0 = disable, logic 1 = enable.
15	D1_2	2dB Attenuator Logic Input, Path 2. Logic 0 = disable, logic 1 = enable.
16	D2_2	4dB Attenuator Logic Input, Path 2. Logic 0 = disable, logic 1 = enable.
17	D3_2	8dB Attenuator Logic Input, Path 2. Logic 0 = disable, logic 1 = enable.
18	D_ATT_OUT_2	5-Bit Digital Attenuator Output (50Ω), Path 2. Requires a DC-blocking capacitor. Connect to A_ATT_IN_2 through a 1000pF capacitor.
19	D4_2	16dB Attenuator Logic Input, Path 2. Logic 0 = disable, logic 1 = enable.
20	A_ATT_IN_2	Analog Attenuator Input (50Ω), Path 2. Requires a DC-blocking capacitor. Connect to D_ATT_OUT_2 through a 1000pF capacitor.
21	DA_SP	Digital Attenuator Serial/Parallel Control Select. Set DA_SP to logic 1 to select serial control. Set DA_SP to logic 0 to select parallel control.
22	A_VCTL_2	Analog Attenuator Voltage Control Input, Path 2. Bypass to ground with a 150pF capacitor if on-chip DAC is used (AA_SP = 1).
23	A_ATT_OUT_2	Analog Attenuator Output (50Ω), Path 2. Requires a DC-blocking capacitor. Connect to AMP_IN_2 through a 1000pF capacitor.
24	$V_{CC\_AMP\_2}$	Driver Amplifier Supply Voltage Input, Path 2. Bypass with a 10nF capacitor as close as possible to the pin.
26	AMP_IN_2	Driver Amplifier Input (50Ω), Path 2. Requires a DC-blocking capacitor. Connect to A_ATT_OUT_2 through a 1000pF capacitor.
27	PD_2	Power-Down, Path 2. See Table 2 for operation details.
29	AMP_OUT_2	Driver Amplifier Output (50Ω), Path 2. Connect a pullup inductor from AMP_OUT_2 to $V_{CC\_}$.
30	REG_OUT	Regulator Output. Bypass with 1µF capacitor.
31	AMPSET	Driver Amplifier Bias Setting for 3.3V Operation. Set to logic 1 for 3.3V operation on pins $V_{CC\_AMP\_1}$ and $V_{CC\_AMP\_2}$. Set to logic 0 for 5V operation.
32	AMP_OUT_1	Driver Amplifier Output (50Ω), Path 1. Connect a pullup inductor from AMP_OUT_1 to $V_{CC\_}$.
34	PD_1	Power-Down, Path 1. See Table 2 for operation details.
35	AMP_IN_1	Driver Amplifier Input (50Ω), Path 1. Requires a DC-blocking capacitor. Connect to A_ATT_OUT_1 through a 1000pF capacitor.
37	$V_{CC\_AMP\_1}$	Driver Amplifier Supply Voltage Input, Path 1. Bypass with a 10nF capacitor as close as possible to the pin.
38	A_ATT_OUT_1	Analog Attenuator Output (50Ω), Path 1. Requires a DC-blocking capacitor. Connect to AMP_IN_1 through a 1000pF capacitor.
39	A_VCTL_1	Analog Attenuator Voltage Control Input, Path 1. Bypass to ground with a 150pF capacitor if on-chip DAC is used (AA_SP = 1).

Pin Description (continued)

PIN	NAME	FUNCTION
40	AA_SP	DAC Enable/Disable Logic Input for Analog Attenuators. Set AA_SP to logic 1 to enable on-chip DAC circuit and digital SPI control. Set AA_SP to logic 0 to disable DAC circuit and digital SPI control. When AA_SP = 0, use analog control lines (A_VCTL_1 and A_VCTL_2).
41	A_ATT_IN_1	Analog Attenuator Input (50Ω), Path 1. Requires a DC-blocking capacitor. Connect to D_ATT_OUT_1 through a 1000pF capacitor.
42	D4_1	16dB Attenuator Logic Input, Path 1. Logic 0 = disable, logic 1 = enable.
43	D_ATT_OUT_1	5-Bit Digital Attenuator Output (50Ω), Path 1. Requires a DC-blocking capacitor. Connect to A_ATT_IN_1 through a 1000pF capacitor.
44	D3_1	8dB Attenuator Logic Input, Path 1. Logic 0 = disable, logic 1 = enable.
45	D2_1	4dB Attenuator Logic Input, Path 1. Logic 0 = disable, logic 1 = enable.
46	D1_1	2dB Attenuator Logic Input, Path 1. Logic 0 = disable, logic 1 = enable.
47	D0_1	1dB Attenuator Logic Input, Path 1. Logic 0 = disable, logic 1 = enable.
—	EP	Exposed Pad. Internally connected to GND. Connect to GND for proper RF performance and enhanced thermal dissipation.

Detailed Description

The MAX2062 high-linearity analog/digital VGA is a general-purpose, high-performance amplifier designed to interface with 50Ω systems operating in the 50MHz to 1000MHz frequency range.

Each channel of the device integrates one digital attenuator and one analog attenuator to provide 64dB of total gain control, as well as a driver amplifier optimized to provide high gain, high IP3, low NF, and low power consumption.

Each digital attenuator is controlled as a slave peripheral using either the SPI-compatible interface, or a 5-bit parallel bus with 31dB total adjustment range in 1dB steps. An added feature allows rapid-fire gain selection among each of the four steps, preprogrammed by the user through the SPI-compatible interface. A separate 2-pin control lets the user quickly access any one of four customized attenuation states without reprogramming the SPI bus. Each analog attenuator is controlled using an external voltage or through the SPI-compatible interface using an on-chip 8-bit DAC. See the *Applications Information* section for attenuator programming details.

Because each of the three stages in the separate signal paths has its own RF input and RF output, this component can be configured to either optimize NF (amplifier configured first), OIP3 (amplifier last), or a compromise of NF and OIP3. The device's performance features include 24dB amplifier gain (amplifier only), 7.3dB NF at maximum gain (includes attenuator insertion losses), and a high OIP3 level of +41dBm. Each of these features makes the device an ideal VGA for multipath receiver and transmitter applications.

In addition, the device operates from a single +5V supply with full performance, or a +3.3V supply for an enhanced power-savings mode with lower performance. The device is available in a compact 48-pin TQFN package (7mm x 7mm) with an exposed pad. Electrical performance is guaranteed over the extended temperature range (T_C = -40°C to +85°C).

Analog and 5-Bit Digital Attenuator Control

The device integrates two analog attenuators and two 5-bit digital attenuators to achieve a high level of dynamic range. Each analog attenuator has a 33dB range and is controlled using an external voltage or through the 3-wire SPI interface using an on-chip 8-bit DAC. Each digital attenuator has a 31dB control range, a 1dB step size, and is programmed either through the 3-wire SPI or through a separate 5-bit parallel bus. See the *Applications Information* section and Table 1 for attenuator programming details. The attenuators can be used for both static and dynamic power control.

Note that when the analog attenuators are controlled by the DACs through the SPI bus, the DAC output voltage shows on pins A_VCTL_1 and A_VCTL_2 (pins 39 and 22, respectively). Therefore, in SPI mode, the A_VCTL_1 and A_VCTL_2 pins must only connect to the resistor and capacitor to ground, as shown in the *Typical Application Circuit*.

Table 1. Control Logic

AA_SP	ANALOG ATTENUATOR	D/A CONVERTER
0	Controlled by external control voltage	Disabled
1	Controlled by on-chip DAC	Enabled (DAC output voltage shows on A_VCTL__ pins); DAC uses on-chip voltage reference
DA_SP	**DIGITAL ATTENUATOR**	
0	Parallel controlled	
1	SPI controlled (control voltages show up on the parallel control pins)	

Driver Amplifier

Each path of the device includes a high-performance driver with a fixed gain of 24dB. The driver amplifier circuits are optimized for high linearity for the 50MHz to 1000MHz frequency range.

Applications Information

Operating Modes

The device features an optional +3.3V supply voltage operation with reduced linearity performance. The AMPSET pin needs to be biased accordingly in each mode, as listed in Table 2. In addition, the driver amplifiers can be shut down independently to conserve DC power. See the biasing scheme outlined in Table 2 for details.

SPI Interface and Attenuator Settings

The digital attenuators can be programmed through the 3-wire SPI/MICROWIRE®-compatible serial interface using 5-bit words. Fifty-six bits of data are shifted in MSB first and are framed by $\overline{CS}$. The first 28 bits set the first attenuator and the following 28 bits set the second attenuator. When $\overline{CS}$ is low, the clock is active and data is shifted on the rising edge of the clock. When $\overline{CS}$ transitions high, the data is latched and the attenuator setting changes (Figure 1). See Table 3 for details on the SPI data format.

Table 2. Operating Modes

RESULT	V_{CC} (V)	AMPSET	PD_1	PD_2
All on	5	0	0	0
	3.3	1	0	0
AMP1 off AMP2 on	5	0	1	0
	3.3	1	1	0
AMP1 on AMP2 off	5	0	0	1
	3.3	1	0	1
All off	5	0	1	1
	3.3	1	1	1

Path 1 DAC and Digital Attenuator Programming

D0:D7 Sent to DAC register
D0 = LSB, D7 = MSB

D8:D12 Preprogrammed Attenuation State 1
D8 = 1dB bit, D9 = 2dB Bit, D10 = 4dB bit, D11 = 8dB bit, D12 = 16dB bit

D13:D17 Preprogrammed Attenuation State 2
D13 = 1dB bit, D14 = 2dB bit, D15 = 4dB bit, D16 = 8dB bit, D17 = 16dB bit

D18:D22 Preprogrammed Attenuation State 3
D18 = 1dB bit, D19 = 2dB bit, D20 = 4dB bit, D21 = 8dB bit, D22 = 16dB bit

D23:D27 Preprogrammed Attenuation State 4
D23 = 1dB bit, D24 = 2dB bit, D25 = 4dB bit, D26 = 8dB bit, D27 = 16dB bit

Path 2 DAC and Digital Attenuator Programming

D28:D35 Sent to DAC register
D28 = LSB, D35 = MSB

D36:D40 Preprogrammed Attenuation State 1
D36 = 1dB bit, D37 = 2dB bit, D38 = 4dB bit, D39 = 8dB bit, D40 = 16dB bit

D41:D45 Preprogrammed Attenuation State 2
D41 = 1dB bit, D42 = 2dB bit, D43 = 4dB bit, D44 = 8dB bit, D45 = 16dB bit

D46:D50 Preprogrammed Attenuation State 3
D46 = 1dB bit, D47 = 2dB bit, D48 = 4dB bit, D49 = 8dB bit, D50 = 16dB bit

D51:D55 Preprogrammed Attenuation State 4
D51 = 1dB bit, D52 = 2dB bit, D53 = 4dB bit, D54 = 8dB bit, D55 = 16dB bit

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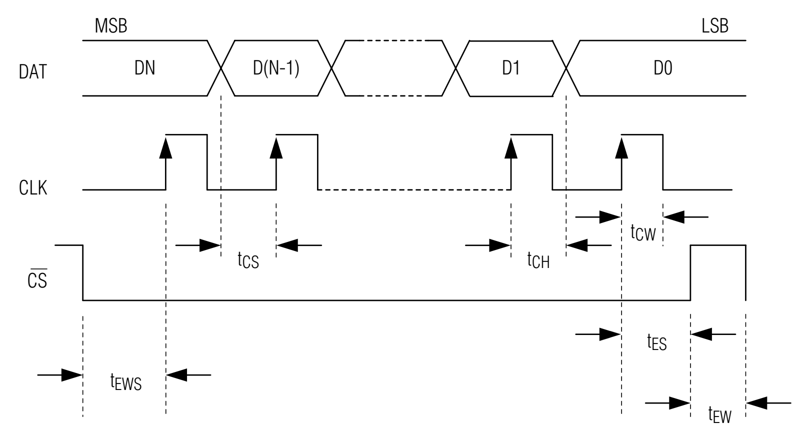
Table 3. SPI Data Format

FUNCTION	BIT	DESCRIPTION
Digital Attenuator State 4 (Path 2)	D55 (MSB)	16dB step (MSB of the 5-bit word used to program the Path 2 digital attenuator state 4)
	D54	8dB step
	D53	4dB step
	D52	2dB step
	D51	1dB step
Digital Attenuator State 3 (Path 2)	D50	16dB step (MSB of the 5-bit word used to program the Path 2 digital attenuator state 3)
	D49	8dB step
	D48	4dB step
	D47	2dB step
	D46	1dB step
Digital Attenuator State 2 (Path 2)	D45	16dB step (MSB of the 5-bit word used to program the Path 2 digital attenuator state 2)
	D44	8dB step
	D43	4dB step
	D42	2dB step
	D41	1dB step
Digital Attenuator State 1 (Path 2)	D40	16dB step (MSB of the 5-bit word used to program the Path 2 digital attenuator state 1)
	D39	8dB step
	D38	4dB step
	D37	2dB step
	D36	1dB step
On-Chip DAC (Path 2)	D35	Bit 7 (MSB) of on-chip DAC used to program the Path 2 analog attenuator
	D34	Bit 6 of DAC
	D33	Bit 5 of DAC
	D32	Bit 4 of DAC
	D31	Bit 3 of DAC
	D30	Bit 2 of DAC
	D29	Bit 1 of DAC
	D28	Bit 0 (LSB) of DAC
Digital Attenuator State 4 (Path 1)	D27	16dB step (MSB of the 5-bit word used to program the Path 1 digital attenuator state 4)
	D26	8dB step
	D25	4dB step
	D24	2dB step
	D23	1dB step
Digital Attenuator State 3 (Path 1)	D22	16dB step (MSB of the 5-bit word used to program the Path 1 digital attenuator state 3)
	D21	8dB step
	D20	4dB step
	D19	2dB step
	D18	1dB step

Table 3. SPI Data Format (continued)

FUNCTION	BIT	DESCRIPTION
Digital Attenuator State 2 (Path 1)	D17	16dB step (MSB of the 5-bit word used to program the Path 1 digital attenuator state 2)
	D16	8dB step
	D15	4dB step
	D14	2dB step
	D13	1dB step
Digital Attenuator State 1 (Path 1)	D12	16dB step (MSB of the 5-bit word used to program the Path 1 digital attenuator state 1)
	D11	8dB step
	D10	4dB step
	D9	2dB step
	D8	1dB step
On-Chip DAC (Path 1)	D7	Bit 7 (MSB) of on-chip DAC used to program the Path 1 analog attenuator
	D6	Bit 6 of DAC
	D5	Bit 5 of DAC
	D4	Bit 4 of DAC
	D3	Bit 3 of DAC
	D2	Bit 2 of DAC
	D1	Bit 1 of DAC
	D0 (LSB)	Bit 0 (LSB) of DAC



NOTES: DATA ENTERED ON CLOCK RISING EDGE.
ATTENUATOR REGISTER STATE CHANGE ON CS RISING EDGE.
N = NUMBER OF DATA BITS.

Figure 1. SPI Timing Diagram

Attenuator and DAC Operation

The two analog attenuators are controlled by an external control voltage applied at A_VCTL_1 and A_VCTL_2 (pins 39 and 22) or by the on-chip 8-bit DACs, while the digital attenuators are controlled through the SPI-compatible interface or through two independent, parallel 5-bit buses. The DAC enable/disable logic-input pin (AA_SP) and digital attenuator SPI/parallel control selection logic-input pin (DA_SP) determine how the attenuators are controlled.

Digital Attenuator Settings Using the Parallel Control Bus

To capitalize on its fast 25ns switching capability, the device offers a supplemental 5-bit parallel control interface. The digital logic attenuator control pins (D0_–D4_) enable the attenuator stages (see Tables 3 and 4).

Direct access to these 5-bit buses enables the user to avoid any programming delays associated with the SPI interface. One of the limitations of any SPI bus is the speed at which commands can be clocked into each peripheral device. By offering direct access to the 5-bit parallel interface, the user can quickly shift between digital attenuator states needed for critical fast-attack automatic gain control (AGC) applications.

Note that when the digital attenuators are controlled by the SPI bus, the control voltages of each digital attenuator appears on the five parallel control pins (pins 14–17 and 19 for digital attenuator 2, pins 42 and 44–47 for digital attenuator 1). **When the digital attenuators are in SPI mode, the parallel control pins must be left unconnected.**

Rapid-Fire Preprogrammed Attenuation States

The device has an added feature that provides rapid-fire gain selection among four preprogrammed attenuation steps. As with the supplemental 5-bit buses previously mentioned, this rapid-fire gain selection allows the user to quickly access any one of four customized digital attenuation states without incurring the delays associated with reprogramming the device through the SPI bus.

The switching speed is comparable to that achieved using the supplemental 5-bit parallel buses. However, by employing this specific feature, the digital attenuator I/O is further reduced by a factor of either 5 or 2.5 (5 control bits vs. 1 or 2, respectively), depending on the number of states desired.

The user can employ the STA_A_1 and STA_B_1 (STA_A_2 and STA_B_2 for digital attenuator 2) logic-input pins to apply each step as required (see Tables 5 and 6). Toggling just the STA_A_1 pin (1 control bit) yields two preprogrammed attenuation states; toggling both the STA_A_1 and STA_B_1 pins together (2 control bits) yields four preprogrammed attenuation states.

Table 4. Digital Attenuator Settings (Parallel Control, DA_SP = 0)

INPUT	LOGIC = 0 (OR GROUND)	LOGIC = 1
D0	Disable 1dB attenuator	Enable 1dB attenuator
D1	Disable 2dB attenuator	Enable 2dB attenuator
D2	Disable 4dB attenuator	Enable 4dB attenuator
D3	Disable 8dB attenuator	Enable 8dB attenuator
D4	Disable 16dB attenuator	Enable 16dB attenuator

Table 5. Programmed Attenuation State Settings for Attenuator 1 (DA_SP = 1)

STA_A_1	STA_B_1	SETTING FOR DIGITAL ATTENUATOR 1*
0	0	Preprogrammed attenuation state 1
1	0	Preprogrammed attenuation state 2
0	1	Preprogrammed attenuation state 3
1	1	Preprogrammed attenuation state 4

**Defined by SPI programming bits D8:D27 (see Table 3 for details).*

Table 6. Programmed Attenuation State Settings for Attenuator 2 (DA_SP = 1)

STA_A_2	STA_B_2	SETTING FOR DIGITAL ATTENUATOR 2**
0	0	Preprogrammed attenuation state 1
1	0	Preprogrammed attenuation state 2
0	1	Preprogrammed attenuation state 3
1	1	Preprogrammed attenuation state 4

***Defined by SPI programming bits D36:D55 (see Table 3 for details).*

Dual 50MHz to 1000MHz High-Linearity, Serial/Parallel-Controlled Analog/Digital VGA

As an example, assume that the AGC application requires a static attenuation adjustment to trim out gain inconsistencies within a receiver lineup. The same AGC circuit can also be called upon to dynamically attenuate an unwanted blocker signal that could desensitize the receiver and lead to an ADC overdrive condition. In this example, the device would be preprogrammed (through the SPI bus) with two customized attenuation states—one to address the static gain-trim adjustment, the second to counter the unwanted blocker condition.

Toggling just the STA_A_1 control bit enables the user to switch quickly between the static and dynamic attenuation settings with only one I/O pin.

If desired, the user can also program two additional attenuation states by using the STA_B_1 control bit as a second I/O pin. These two additional attenuation settings are useful for software-defined radio applications where multiple static gain settings are needed to account for different frequencies of operation, or where multiple dynamic attenuation settings are needed to account for different blocker levels (as defined by multiple wireless standards).

Power-Supply Sequencing

The sequence to be used is:

1) Power supply
2) Control lines

Layout Considerations

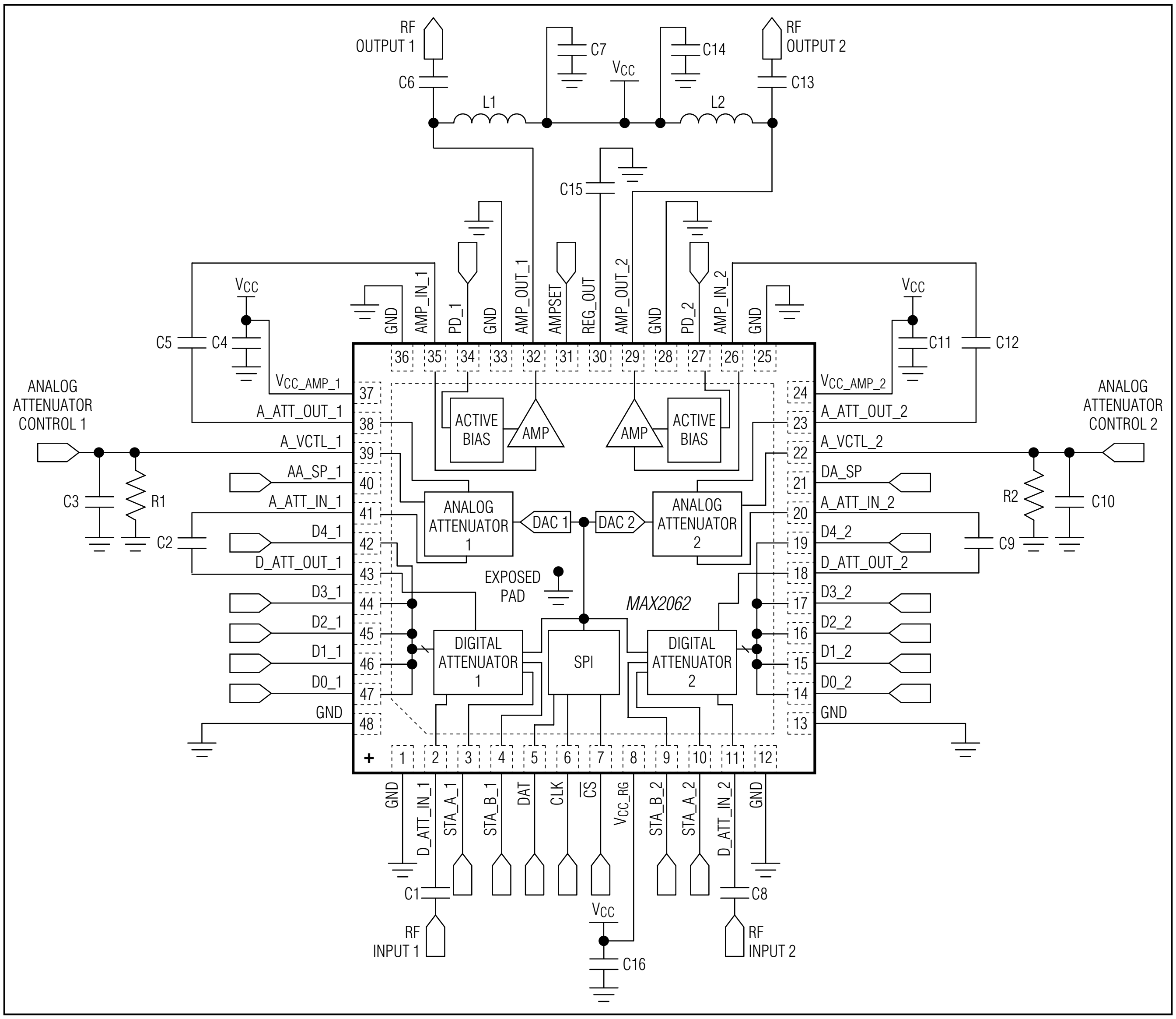
The pin configuration of the device is optimized to facilitate a very compact physical layout of the device and its associated discrete components. The exposed pad (EP) of the device's 48-pin TQFN-EP package provides a low thermal-resistance path to the die. It is important that the PCB on which the device is mounted be designed to conduct heat from the EP. In addition, provide the EP with a low inductance path to electrical ground. The EP **MUST** be soldered to a ground plane on the PCB, either directly or through an array of plated via holes. The layout of the PCB should include proper top-layer ground shielding to isolate the amplifier's inputs and outputs from each other. Shielding between the paths (inputs and outputs) is important for channel-to-channel isolation.

Table 7. Typical Application Circuit Component Values

DESIGNATION	QTY	DESCRIPTION	COMPONENT SUPPLIER
C1, C2, C5, C6, C8, C9, C12, C13	8	1000pF ceramic capacitors (0402) GRM1555C1H102J	Murata Electronics North America, Inc.
C3, C10	2	150pF ceramic capacitors (0402) GRM1555C1H151J	Murata Electronics North America, Inc.
C4, C7, C11, C14, C16	5	10nF ceramic capacitors (0402) GRM155R71E103K	Murata Electronics North America, Inc.
C15	1	1µF ceramic capacitor (0603) GRM188R71C105K	Murata Electronics North America, Inc.
L1, L2*	2	820nH inductors (1008) Coilcraft 1008CS-821XJLC	Coilcraft, Inc.
R1, R2	2	47.5kΩ resistors (0402)	—
U1	1	48 TQFN-EP (7mm x 7mm) Maxim MAX2062ETM	Maxim Integrated Products, Inc.

**Select the inductors to ensure that self-resonance of the inductors is outside the band of operation.*

Typical Application Circuit



Chip Information

PROCESS: SiGe BiCMOS

Package Information

For the latest package outline information and land patterns, go to. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
48 TQFN-EP	T4877+7	21-0144	90-0133

Dual 50MHz to 1000MHz High-Linearity, Serial/Parallel-Controlled Analog/Digital VGA

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/10	Initial release	—
1	11/10	Updated *Output Voltage* specification	5
2	8/15	Removed military reference from *Applications*	1