P-Channel Enhancement Mode Field Effect Transistor

General Features		
V_{DSS}	I_D	$R_{DS(ON)}$ (m) Typ
-30V	-55A	10 @ VGS=-10.0V
		15 @ VGS=-4.5V

DESCRIPTION

The MSH3509 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch

MSH3509
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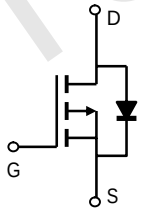

P-DFN3X3 top and bottom view **Marking and pin Assignment** **Schematic diagram**

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [A]	T_A=25°C	I_D	-55	A
	T_A=70°C		-38	
Pulsed Drain Current [B]		I_{DM}	-180	
Power Dissipation [A]	T_A=25°C	P_D	50	W
	T_A=70°C		35	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics					
Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	45	62	°C/W
Maximum Junction-to-Ambient [A]	Steady-State		54	75	°C/W
Maximum Junction-to-Lead [C]	Steady-State	$R_{\theta JL}$	21	30	°C/W

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Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0, I_D=-250μA	-30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250μA	1		3	V
I_{GSS}	Gate Body Leakage	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-30V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS}=-10V, I_D= -30A		10	12	mΩ
		V_{GS}=-4.5V, I_D=-15A		15	17	
V_{SD}	Diode Forward Voltage	I_S=-2.7A, V_{GS}=0V		0.7		V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=-15V, V_{GS}=-4.5V,I_D=-15A		33		nC
Qgs	Gate-Source Charge	V_{DS}=-15V,		11		
Qgd	Gate-Drain Charge	V_{GS}=-4.5V,I_D=-15A		13		
Ciss	Input capacitance	V_{DS}=-15V, V_{GS}=0V, f=1MHz		3500		pF
Coss	Output Capacitance			510		
Crss	Reverse Transfer Capacitance			420		
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=-15V, R_L =15Ω		8		ns
t_r	Turn-On Rise Time	I_D=-15A , V_{GEN}=-10V		18		
$t_{d(off)}$	Turn-Off Delay Time	R_G=3Ω		78		
t_f	Turn-Off Fall Time			42		

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design. The current rating is based on the t≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

D. The static characteristics in Figures 1 to 6,12,14 are obtained using 80μs pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

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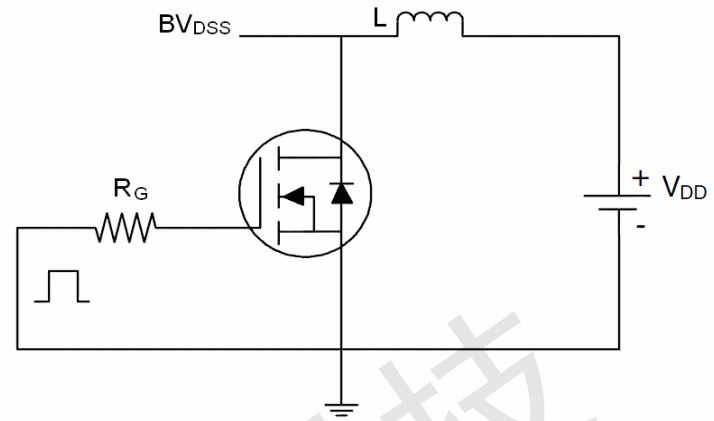
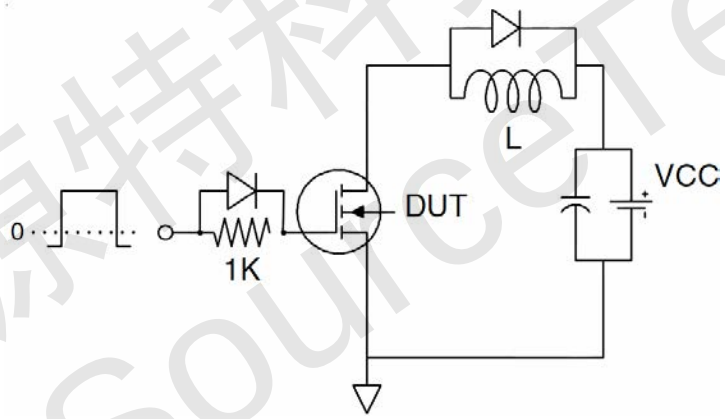
Test Circuit

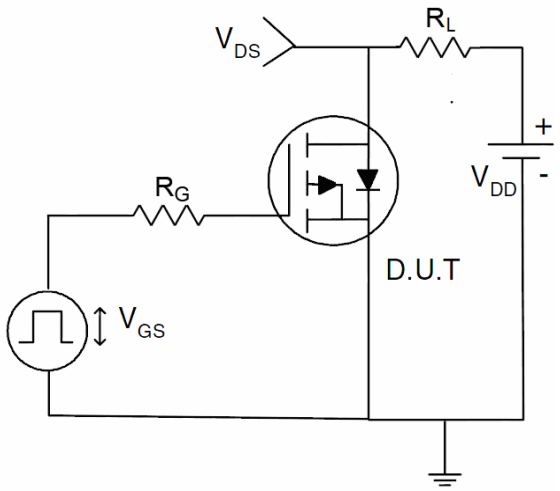
1) E_{AS} Test Circuits



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

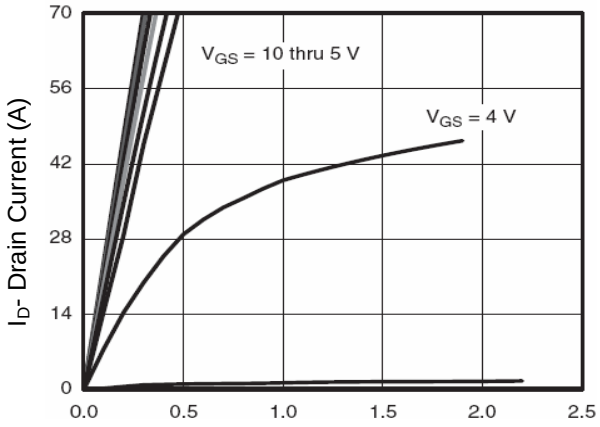


Figure 1 Output Characteristics

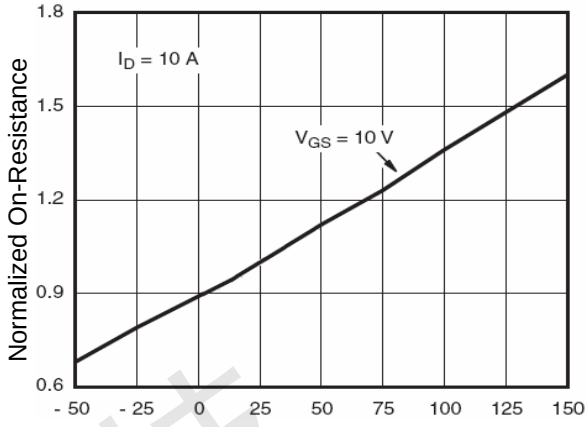


Figure 4 Rdson-Junction Temperature

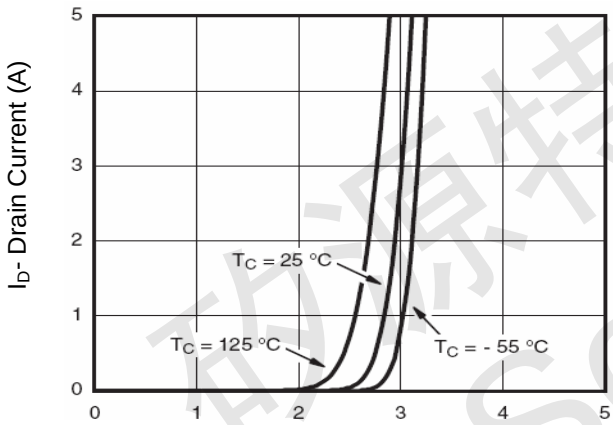


Figure 2 Transfer Characteristics

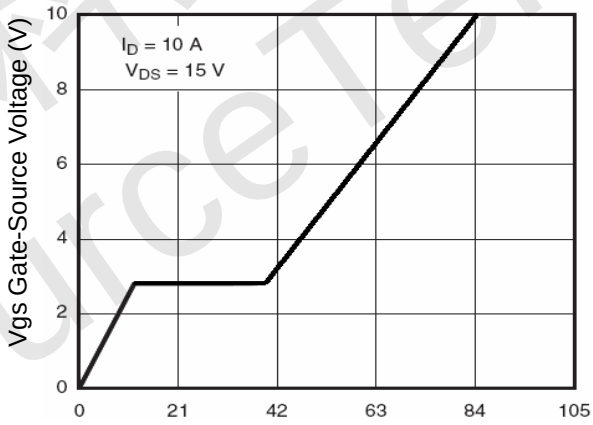


Figure 5 Gate Charge

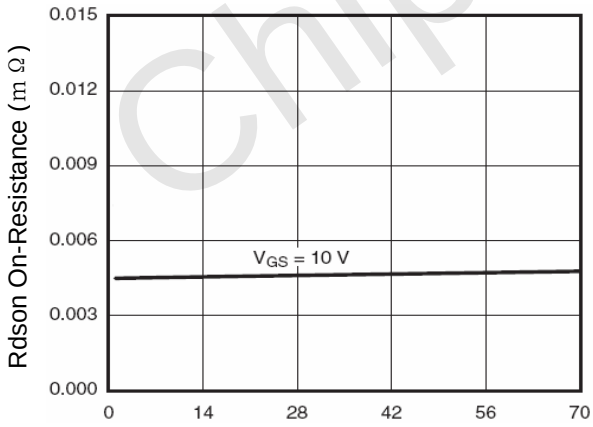


Figure 3 Rdson- Drain Current

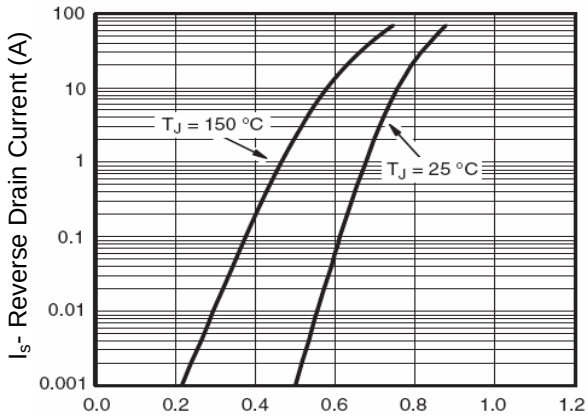


Figure 6 Source- Drain Diode Forward

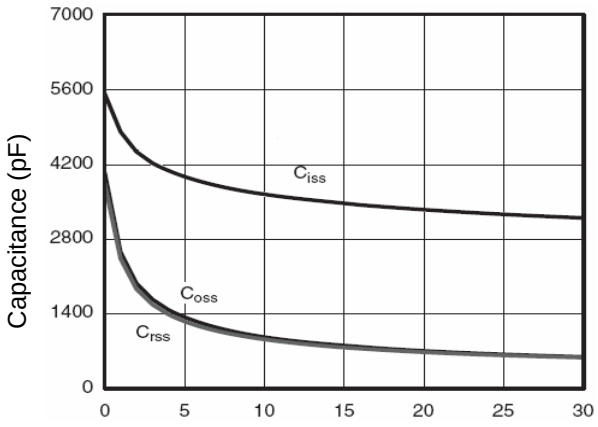
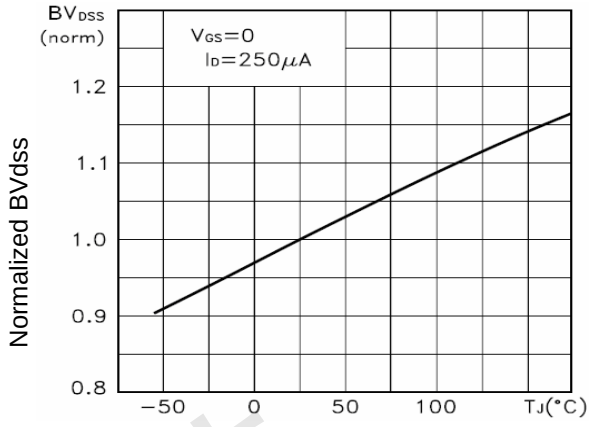


Figure 7 Capacitance vs Vds



TJ-Junction Temperature(℃)

Figure 9 BV_{DSS} vs Junction Temperature

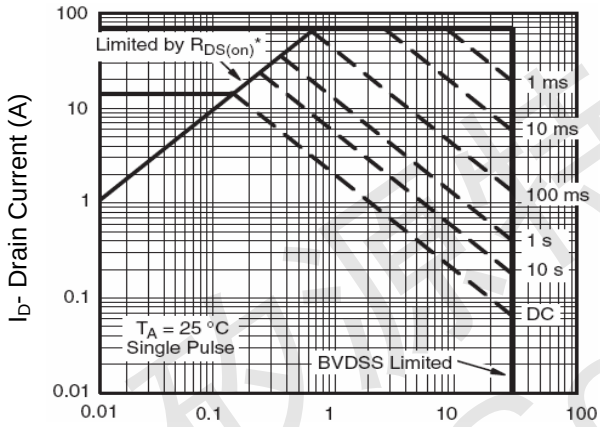


Figure 8 Safe Operation Area

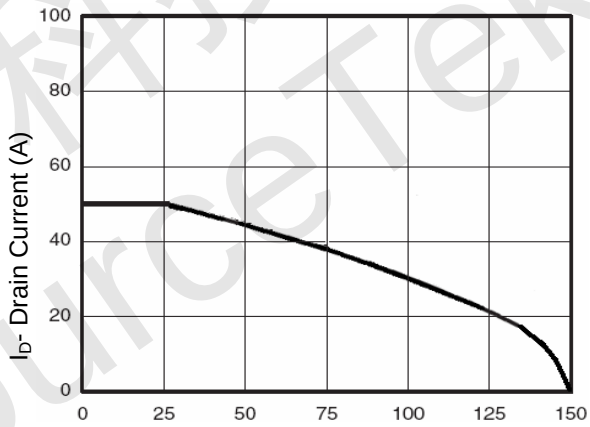
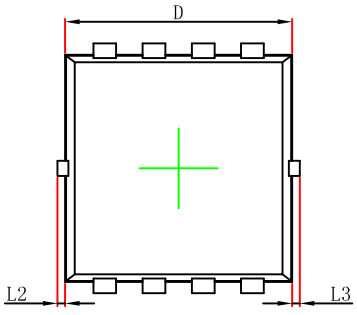


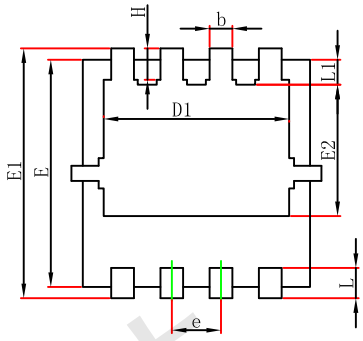
Figure 10 ID Current Derating vs Junction Temperature

Figure 11 Normalized Maximum Transient Thermal Impedance

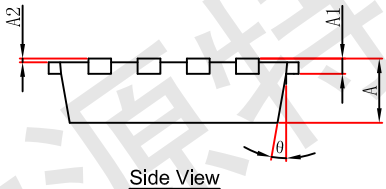
PDFNWB(3×3)-8L PACKAGE OUTLINE DIMENSIONS



Top View
[顶视图]



Bottom View
[背视图]



Side View
[侧视图]

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.650	0.850	0.026	0.033
A1	0.152 REF.		0.006 REF.	
A2	0~0.05		0~0.002	
D	2.900	3.100	0.114	0.122
D1	2.300	2.600	0.091	0.102
E	2.900	3.100	0.114	0.122
E1	3.150	3.450	0.124	0.136
E2	1.535	1.935	0.060	0.076
b	0.200	0.400	0.008	0.016
e	0.550	0.750	0.022	0.030
L	0.300	0.500	0.012	0.020
L1	0.180	0.480	0.007	0.019
L2	0~0.100		0~0.004	
L3	0~0.100		0~0.004	
H	0.315	0.515	0.012	0.020
θ	9°	13°	9°	13°

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