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NY8L050A

**8-bit 65C02 MCU with 12x55 LCD Driver,
32 I/O, & '1-Ch Speech + Dual-Tone'**

Version 1.0

Nov. 19, 2018

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Revision History

<i>Version</i>	<i>Date</i>	<i>Description</i>	<i>Modified Page</i>
1.0	2018/11/19	Formal release.	-

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1. 概述

NY8L050A 為高性能 8 位元 65C02 微控制器附加LCD驅動和聲音播放功能，三組8位元 timer / counter，32 根 I/O。LCD 驅動單元除控制台功能之外，還內建按鍵偵測功能。

聲音播放功能共有3通道，1個通道可播放語音，其他兩個通道作雙通道音樂，所有通道可以同步播放。播放時使用高音質 ADPCM 合成演算法，播放採樣率可以到 16KHz@4MHz，並支援音量調整，可以組成高品質的聲音播放，NY8L050A提供兩種高精度的音訊輸出方式，一種是10位元DAC輸出，另一種是 9 位元PWM 輸出。

NY8L050A提供4通道，8位元精度ADC功能，適合類比信號的診斷和量測應用。

MCU 為 CISC 架構易於編程和控制以及規劃到多種的應用。此外並提供多種工作模式 Slow mode, Standby mode 及 Halt mode (Sleep Mode) 來有效減少功耗。

2. 功能

- 寬廣的工作電壓範圍：2.0V~5.5V @ System clock \leq 4MHz；3.0V~5.5V @ System clock \leq 8MHz。
- 128K-Byte ROM，程式和語音共用。
- 320-Byte RAM。
- LCD 點數 (COM x SEG)：12 x 55。
- 32 GPIO，其中 22 根和 LCD SEG 共用。
- 雙時脈振盪：系統時鐘可自由選擇高速或低速。
 - 高速振盪: IO8M / IO4M / IO2M / IO500K。
 - 低速振盪: IO32K / XTAL32K。
- 內建高精準振盪線路(+/- 1.5%)。
- 四種工作模式可有效省電減少功耗：
 - Normal mode、Slow mode、Standby mode 及 Halt mode。
- Normal mode 下 CPU clock 速度可程式化：
 - 可設定為高速振盪的 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128。
- 3 組 8 位元 Timer，可應用於語音通道、音頻或 RFC 等等應用。
- 支援大多數 LCD 顯示：
 - 1/2, 1/3, 1/4 bias。
 - 1/4, 1/5, 1/6, 1/8, 1/9, 1/10, 1/11, 1/12 duty。
- 內建 Charge pump 昇壓供應 LCD 顯示。
- COM & SEG 可設定成 LED sink / drive 功能。
- LCD 支援 Matrix key 功能，input & output 起始位置可在組態中設定。
- Serial peripheral interface (SPI) Master mode 可存取 SPI 元件。



- EL 驅動功能，可設定頻率和佔空比。
- RFC 功能，可用於溫度、濕度偵測應用。
- 完整的系統保護，低电压偵測重置功能，Watch-dog reset 看門狗重置功能及external reset pin 外部重置腳。
- 彈性的 I/Os 設定：floating 輸入、pull-low 輸入、CMOS 輸出、open-drain 輸出。
- 紅外線載波頻率可供選擇，同時載波之極性也可以根據數據作選擇。
- 聲音播放功能共有 3 通道，通道 0/1 作音頻、通道 2 可播放語音，所有通道可以同步播放。
- 高音質 4-bit ADPCM 合成演算法。
- 高品質9位元直推PWM輸出和10位元DAC音頻輸出。
- 4通道，8位元精度模拟数字转换功能(ADC)
- 8 種中斷模式。
- 16 階音量輸出控制。
- LCD 點數組合：

COMMON	SEGMENT	DOTS
12	55	660
11	56	616
10	57	570
9	58	522
8	59	472
6	61	366
5	62	310
4	63	252



1. GENERAL DESCRIPTION

NY8L050A is a high-performance 8-bit 65C02 micro-controller with LCD driver and sound processor, three sets of 8-bit timer/counter, 32 general I/Os. For LCD driver, it applies for the most common-used LCD panels and functions as a key strobe for further application.

There are 3 channels that are configured as 1-channel speech and dual-tone melody, and all of them can be auto-played back simultaneously. Not only high fidelity ADPCM speech synthesis algorithm built-in, but also wide range sampling rate up to 16KHz@4MHz and different volume level are supported. Those combinations create remarkable high-quality voice. NY8L050A provides two kinds of audio outputs with fine resolution, one is 10-bit current-type D/A converter (DAC) and the other is 9-bit Pulse-Width-Modulation (PWM).

The NY8L IC provides 4 channels high-precision 8-bit analog-to-digital converter (ADC), which is suitable for any analog interface detection and measurement applications.

The CISC MCU architecture is very easy to program and control, various applications can be easily implemented. Furthermore, in addition to the Slow mode, it offers the Standby mode and Halt mode (Sleep mode) to minimize power dissipation.

2. FEATURES

- Wide operating voltage range: 2.0V~5.5V @ System clock \leq 4MHz; 3.0V~5.5V @ System clock \leq 8MHz.
- 128KB ROM, program and voice data share the same ROM space.
- 320B RAM.
- LCD Dots (COM x SEG): 12 x 55.
- 32 GPIO, 22 shared from LCD SEG.
- Dual-clock oscillation: System clock can switch between high oscillation and low oscillation.
 - High oscillation: IOSC8M / IOSC4M / IOSC2M / IOSC500K.
 - Low oscillation: IOSC32K / XTAL32K.
- Precisely embedded oscillator with build-in resistor (+/- 1.5%).
- Four kinds of operation mode to reduce system power consumption:
 - Normal mode, Slow mode, Standby mode and Halt mode.
- At Normal mode, CPU clock is software programmable.
 - 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128 of high oscillator (F_{FAOS}) frequency.
- Three 8-bit timers for 1-channel speech and 2-channel tone or other applications such as RFC.
- Support most of LCD panel types:
 - 1/2, 1/3, 1/4 bias.
 - 1/4, 1/5, 1/6, 1/8, 1/9, 1/10, 1/11, 1/12 duty.
- Charge pump for the LCD display power.



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- LED sink/drive configuration supported through COM & SEG.
- Matrix key supported, and input & output starting pad can be selected by option.
- Serial peripheral interface (SPI) Master mode for serial Flash/SRAM memory.
- Electroluminescent (EL) back light driver block supported with various frequency and duty.
- Resistance to Frequency Converter (RFC) for the detection of humidity, temperature or other applications.
- Low voltage reset, watch-dog reset (by option) and external reset pin (by option) are all supported to protect the system.
- Flexible I/Os maximum with optional function: floating input, pull-low input, CMOS output, open-drain output.
- Infrared output: optional IR carrier frequency and optional data high/low IR output supported.
- Maximum of 3 channels can play simultaneously; channel0/1 can be assigned as tone, channel2 can be assigned as speech.
- New high fidelity 4-bit ADPCM speech synthesis algorithm.
- High quality direct-drive 9-bit PWM and 10-bit D/A converter audio output
- 4 channels high-precision 8-bit analog-to-digital converter (ADC)
- 8 interrupt modes supported.
- 16 steps volume control for audio output.
- Possible LCD COM and SEG combination:

COMMON	SEGMENT	DOTS
12	55	660
11	56	616
10	57	570
9	58	522
8	59	472
6	61	366
5	62	310
4	63	252



3. BLOCK DIAGRAM

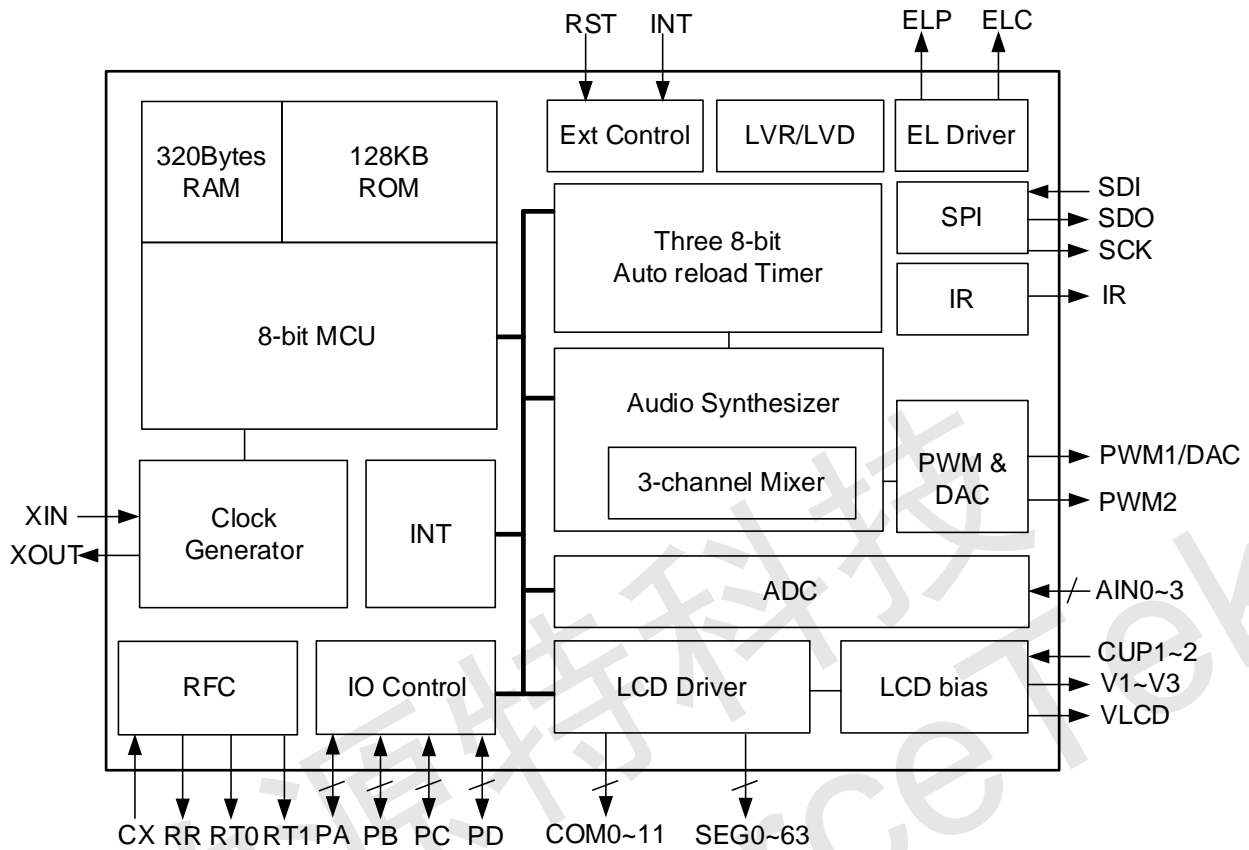


Fig.1-1: The block diagram

4. PAD DESCRIPTION

Pad Name	ATTR.	Description
VDD1~3	P	Positive supply power.
VSS1~3	P	Negative supply power.
PA0/Xin	I/O	Bit 0 for Port A, or input of XTAL32K.
PA1/Xout	I/O	Bit 1 for Port A, or output of XTAL32K.
PA2/INT	I/O	Bit 2 for Port A, or external interrupt input.
PA3/RST	I/O	Bit 3 for Port A, or external reset input.
PA4/CX/AIN3	I/O	Bit 4 for Port A, or input of RFC function, or input port3 of ADC.
PA5/RR/AIN2	I/O	Bit 5 for Port A, or output of RFC function, or input port2 of ADC..
PA6/RT0/AIN1	I/O	Bit 6 for Port A, or output of RFC function, or input port1 of ADC..
PA7/RT1/AIN0	I/O	Bit 7 for Port A, or output of RFC function, or input port0 of ADC..
PB0/PWM2	I/O	Bit 0 for Port B, or PWM2 output.
PB1/PWM1/DAC	I/O	Bit 1 for Port B, or PWM1 output, or DAC output.



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Pad Name	ATTR.	Description
SEG0/PB2/ELP	I/O	LCD segment 0, Bit 2 for Port B, or charging signal of EL driver.
SEG1/PB3/ELC	I/O	LCD segment 1, Bit 3 for Port B, or discharging signal of EL driver.
SEG2/PB4/IR	I/O	LCD segment 2, Bit 4 for Port B, or IR output.
SEG3/PB5/SCK	I/O	LCD segment 3, Bit 5 for Port B, or clock output of SPI.
SEG4/PB6/SDI	I/O	LCD segment 4, Bit 6 for Port B, or data input (MISO) of SPI.
SEG5/PB7/SDO	I/O	LCD segment 5, Bit 7 for Port B, or data output (MOSI) of SPI.
SEG6~13/PC0~7	I/O	LCD segment 6~13, or Bit 0~7 for Port C
SEG14~21/PD0~7	I/O	LCD segment 14~21, or Bit 0~7 for Port D (can be used as key strobe input).
SEG22~54	O	LCD segment 22~54 (SEG22~37 can be used as key strobe output).
COM0~11	O	LCD common 0~11 (COM3~11 can be used as SEG63~55).
V1~3, VLCD	P	LCD supply power.
CUP1~2	I/O	Auxiliary capacitor pins for voltage pumping.

Total : 89 Pins

Legend: I = Input O = Output P = Power



5. OPERATION MODES

NY8L050A provide four kinds of operating mode to tailor all kinds of application and save power consumptions. These operating modes are Normal mode, Slow mode, Standby mode and Halt mode. Normal mode is designated for high-speed operating mode. Slow mode is designated for low-speed mode in order to save power consumption. At Standby mode, NY8L050A will stop almost all operations except Timer2/Timer1/Timer0/FT/ST (based on F_{SLOW}) in order to wake up periodically. At Halt mode, NY8L050A will sleep until Key change or external interrupt occurs. User can set the control register OPMD to swap Normal/Slow mode and the control register SLP to enter Standby/Halt mode.

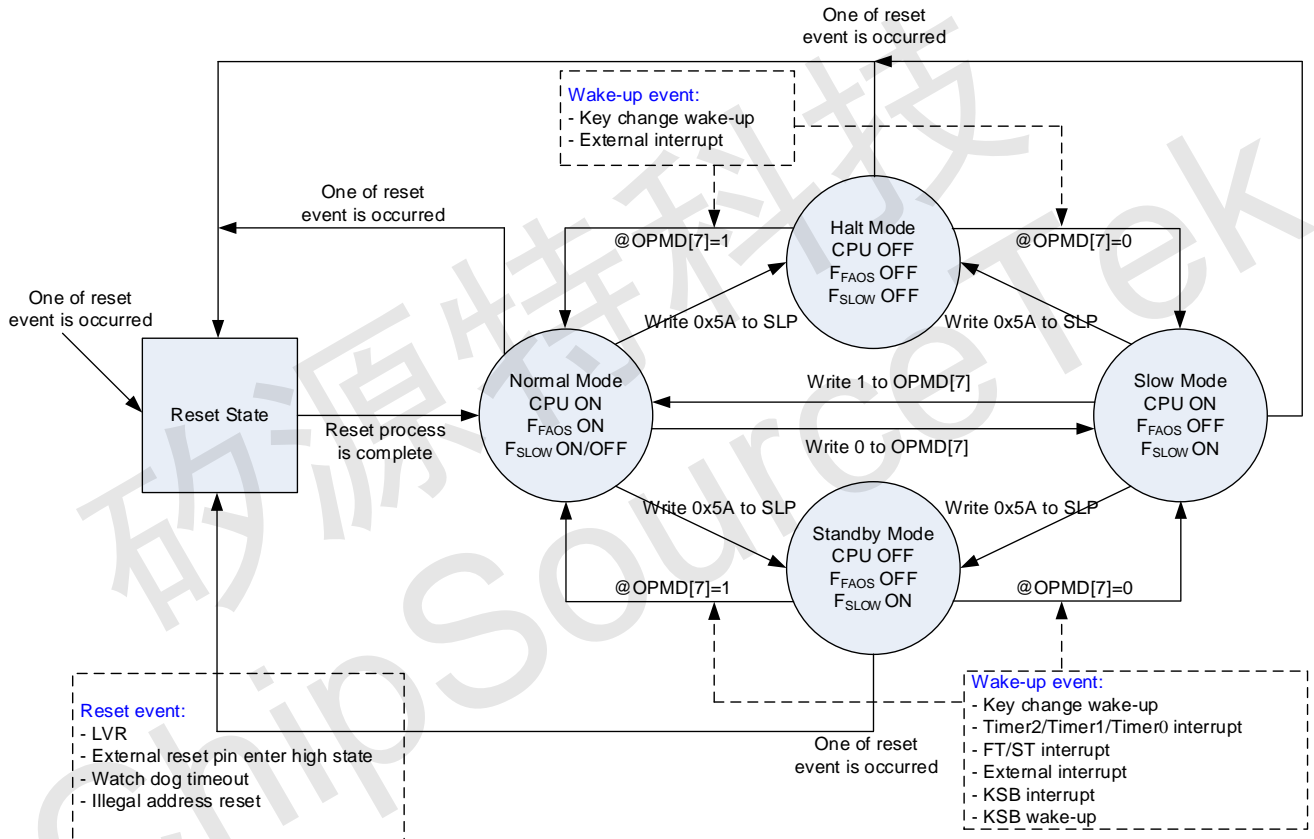


Fig. 5-1: Four Operating Modes



6. LCD WAVEFORMS

The following lists voltage level of corresponding bias settings and users have to connect with the identical power system.

Bias	Voltage Level
1/2	VSS, V1 (1/2*VLCD), VLCD
1/3	VSS, V1 (1/3*VLCD), V2 (2/3*VLCD), VLCD
1/4	VSS, V1 (1/4*VLCD), V2 (2/4*VLCD), V3 (3/4*VLCD), VLCD

The LCD timing waveforms are shown as Fig.6-1 ~ Fig.6-3.

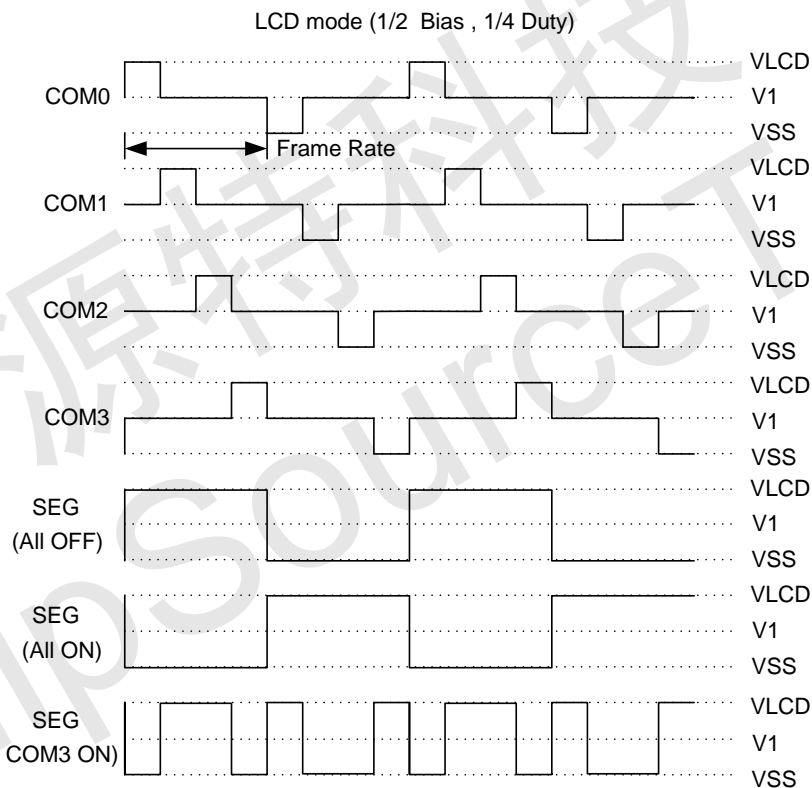


Fig.6-1: LCD timing waveform of 1/2 bias, 1/4 Duty

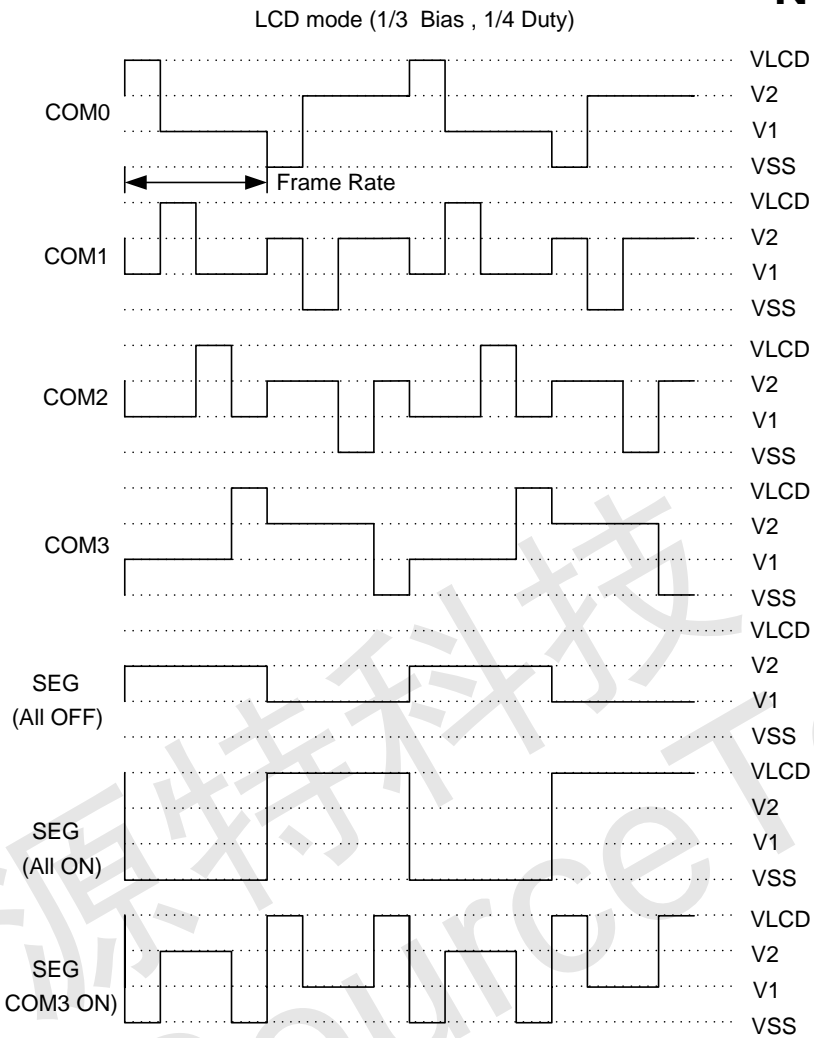


Fig.6-2: LCD timing waveform of 1/3 bias, 1/4 Duty

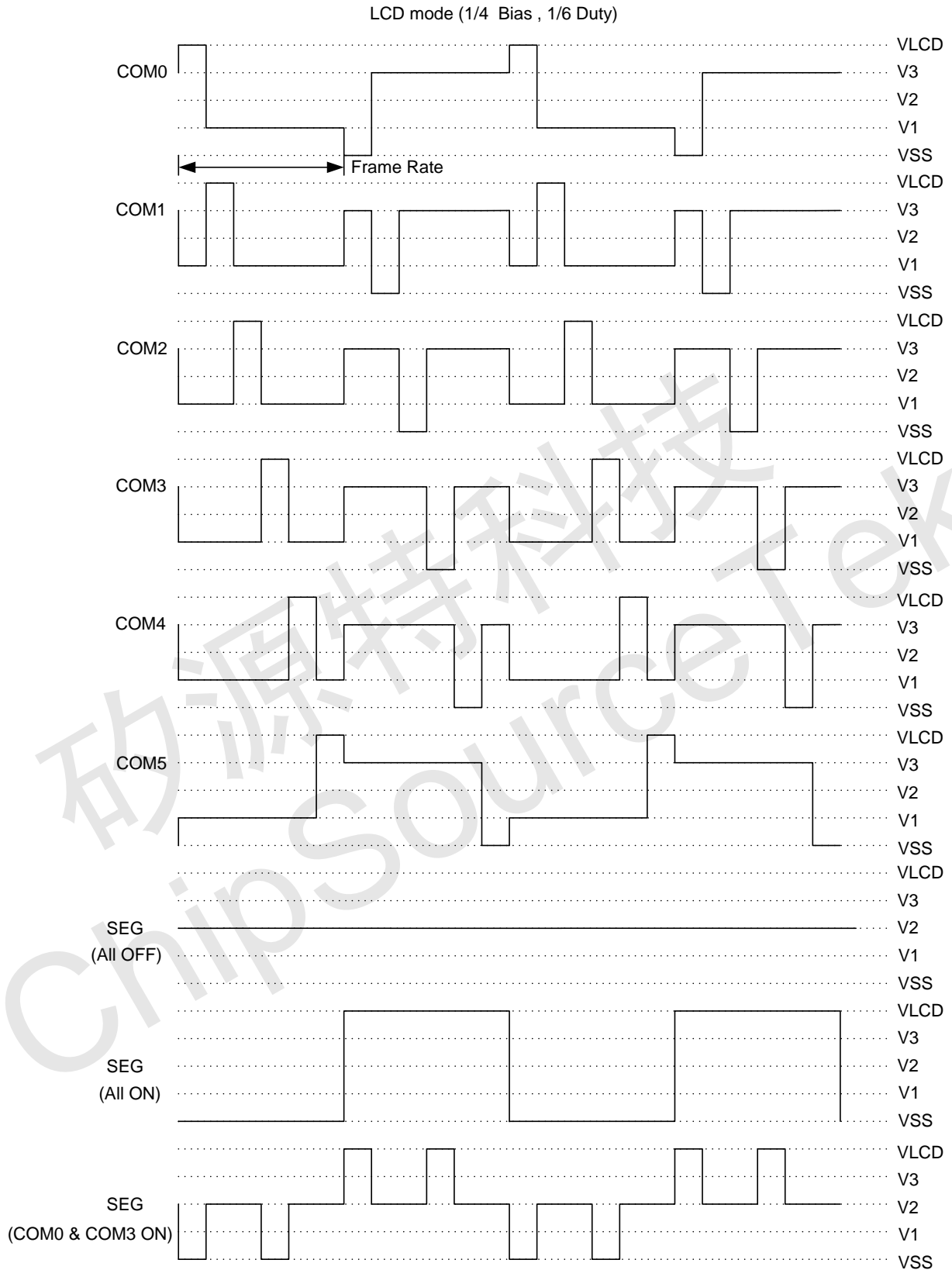


Fig.6-3: LCD timing waveform of 1/4 bias, 1/6 Duty



7. ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Rating

Symbol	Parameter	Rated Value	Unit
VDD - VSS	Supply voltage	-0.5 ~ +6.0	V
Vin	Input voltage	VSS-0.3V ~ VDD+0.3	V
Top	Operating Temperature	0 ~ +70	°C
Tst	Storage Temperature	-25 ~ +85	°C

7.2 DC Characteristics

Symbol	Parameter	VDD	Min.	Typ.	Max.	Unit	Test Condition
V _{DD}	Operating voltage		2.0	3.0	5.5	V	F _{CPU} = 4MHz
			3.0	4.5	5.5		F _{CPU} = 8MHz
I _{HALT}	Halt mode	3 4.5	0.1	0.1	0.5	uA	Sleep, no load
			0.1	0.1	0.5		
I _{SB1}	Standby Mode 1	3 4.5	1.4	1.4	2.8	uA	CPU off, 32KHz on, LCD off, Reg off, no load
			1.4	1.4	2.8		
I _{SB2}	Standby Mode 2	3 4.5	1.5	1.5	3.0	uA	CPU off, 32KHz on, LCD on, Reg off, no load
			1.5	1.5	3.0		
I _{SB3}	Standby Mode 3	3 4.5	5	5	8	uA	CPU off, 32KHz on, LCD on, Reg on, no load
			5	5	8		
I _{SL}	Slow mode	3 4.5	15	15	30	uA	F _{CPU} =32KHz, PWM output off, no load
			15	15	30		
I _{OP}	Normal mode	3 4.5	0.8	0.8	1.8	mA	F _{CPU} =4MHz, PWM output off, no load
			0.8	0.8	1.8		
I _{IH}	Input current (Internal pull-low)	3 4.5 3 4.5	3	3	9	uA	V _{IN} = VDD
			3	3	9		
			30	30	90		
			30	30	90		
I _{OH}	Output high current (PA/B/C/D, SEG/COM@LED mode)	3 4.5	-9	-9	-12	mA	V _{OH} = 2.0V
			-9	-9	-12		V _{OH} = 3.5V
I _{OL1}	Output low current (PA/B/C/D)	3 4.5	18	18	25	mA	V _{OL} = 1.0V
			18	18	25		V _{OL} = 1.0V
I _{OL2}	Output low current (SEG/COM@LED mode)	3 4.5	9	9	12.5	mA	V _{OL} = 1.0V
			9	9	12.5		V _{OL} = 1.0V
I _{PWM}	PWM output current	3 4.5	150	150	250	mA	Load = 8 ohms
			150	150	250		
IDAC	DAC output current	3 4.5	1.4	1.4	1.6	mA	Half scale
			1.4	1.4	1.6		
ΔF/F	Frequency deviation by voltage drop	3 4.5	-0.5	-0.5	-0.5	%	<u>Fosc(3.0V) - Fosc(2.4V)</u> Fosc(3.0v)
			-0.5	-0.5	-0.5		<u>Fosc(4.5V) - Fosc(3.0V)</u> Fosc(4.5v)
ΔF/F	Frequency lot deviation (4MHz)	3	-1.5	1.5	1.5	%	<u>Fosc(3.0V) - 4MHz</u> 4MHz
	Frequency lot deviation (8MHz)	4.5	-1.5	1.5	1.5	%	<u>Fosc(4.5V) - 8MHz</u> 8MHz
Fosc	Oscillation Frequency	--	0.48	0.5	0.52	MHz	V _{DD} = 2.0~5.5V
			1.95	2	2.05		
			3.9	4	4.1		
			7.8	8	8.2		



8. APPLICATION CIRCUITS

8.1 Application Circuits with Low Loading

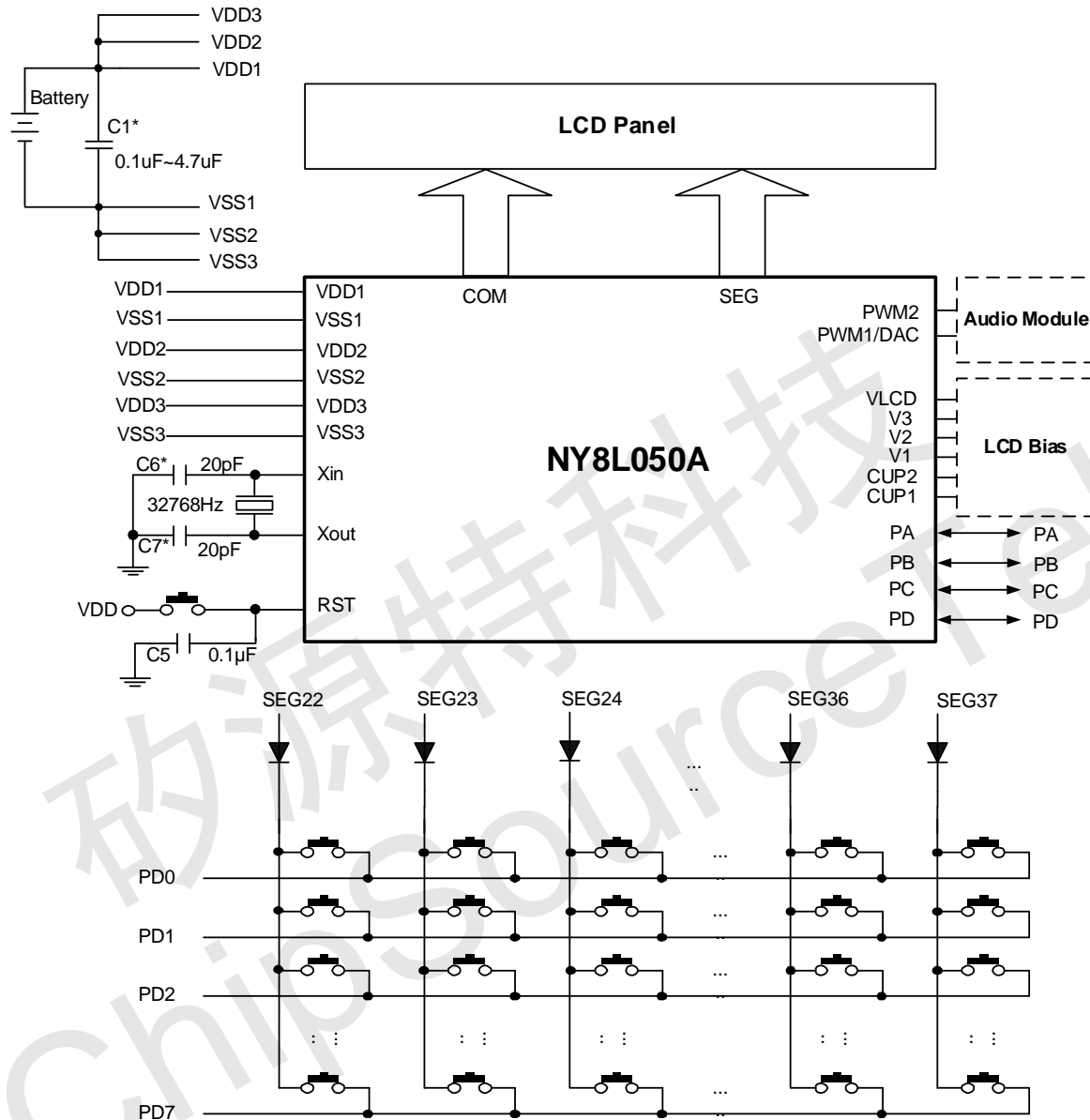


Fig.8-1: The Application Circuits with Low Loading

PCB Layout Guidelines:

1. VDD must be connected to power input port directly, not the branch of each other.
2. VLCD should be higher than or equal to VDD, otherwise will cause large current.
3. VSS must be connected to ground input directly, not the branch of each other.
4. Capacitor (used for XTAL32K) is proposed to be 12~20 pF.
5. C1 is suggested 0.1uF~4.7uF, and should be increased in high volume application.



8.2 Application Circuits with Heavy Loading (Such as Motor, High Brightness LED)

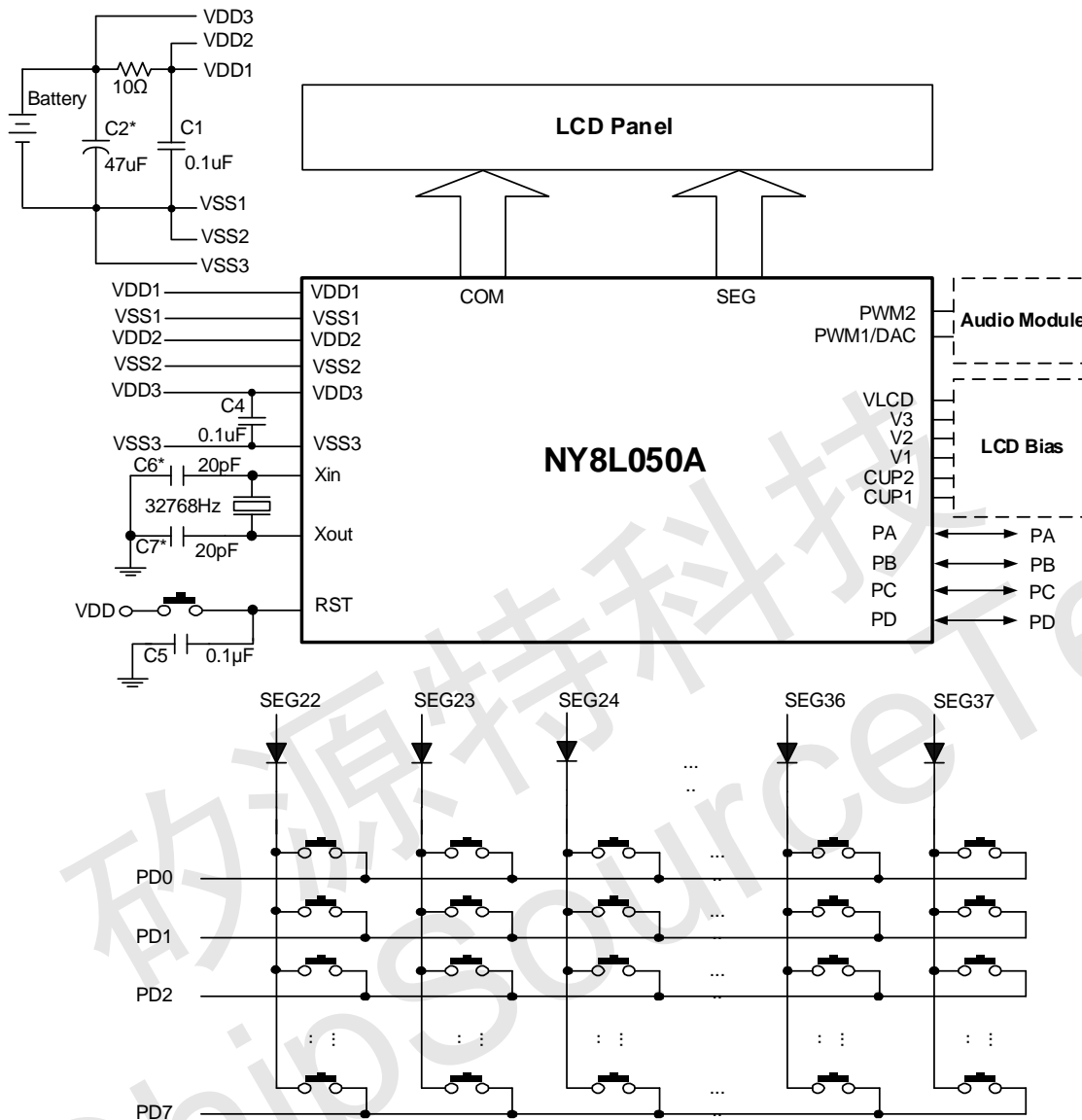


Fig.8-2: The Application Circuits with Heavy Loading

PCB Layout Guidelines:

1. VDD must be connected to power input port directly, not the branch of each other.
2. VLCD should be higher than or equal to VDD, otherwise will cause large current.
3. VSS must be connected to ground input directly, not the branch of each other.
4. Capacitor (used for XTAL32K) is proposed to be 12~20 pF.
5. C2 is suggested 47μF, and should be modified in different loading.



8.3 LCD Bias (VDD for VLCD/V3/V2/V1 or internal Vreg for V1)

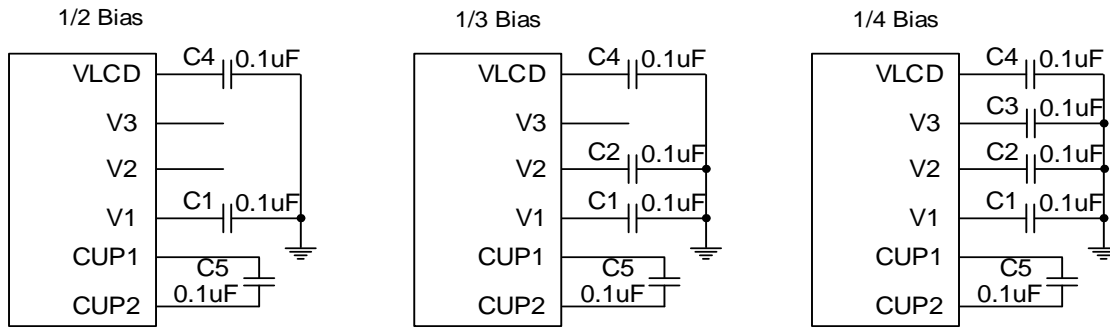


Fig.8-3: The diagram of LCD Bias based on VDD or internal Vreg

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9. DIE PAD DIAGRAM

