



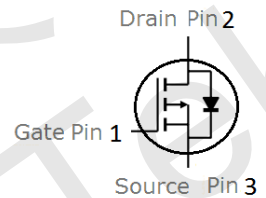
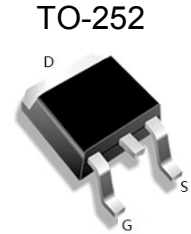
-30V/-50A P-Channel Advanced Power MOSFET

VS3510AD

Features

- P-Channel, -5V Logic Level Control
- Low on-resistance RDS(on) @ VGS=-4.5 V
- Fast Switching
- Enhancement mode
- 100% Avalanche Tested
- Pb-free lead plating; RoHS compliant

V_{DS}	-30	V
$R_{DS(on),TYP@ V_{GS}=-10 V}$	10	mΩ
$R_{DS(on),TYP@ V_{GS}=-4.5V}$	18	mΩ
I_D	-50	A



Part ID	Package Type	Marking	Tape and reel information
VS3510AD	TO-252	3510AD	2500PCS/Reel

Maximum ratings, at T_A=25 °C, unless otherwise specified

Symbol	Parameter	Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage	-30	V
V_{GS}	Gate-Source voltage	±20	V
I_S	Diode continuous forward current	$T_C = 25^\circ C$	-50 A
I_D	Continuous drain current @ $V_{GS} = -10V$	$T_C = 25^\circ C$	-50 A
		$T_C = 100^\circ C$	-36 A
I_{DM}	Pulse drain current tested ①	$T_C = 25^\circ C$	-200 A
I_{DSM}	Continuous drain current @ $V_{GS} = -10V$	$T_A = 25^\circ C$	-8 A
		$T_A = 70^\circ C$	-6 A
EAS	Avalanche energy, single pulsed ②	43	mJ
P_D	Maximum power dissipation	$T_C = 25^\circ C$	52 W
P_{DSM}	Maximum power dissipation ③	$T_A = 25^\circ C$	1.25 W
MSL		Level 3	
$T_{STG} T_J$	Storage and Junction Temperature Range	-55 to 175	°C
Thermal Characteristics			
$R_{\theta JC}$	Thermal Resistance-Junction to Case	2.9	°C/W
$R_{\theta JA}$	Thermal Resistance Junction-Ambient	100	°C/W



Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_J = 25°C (unless otherwise stated)						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250μA	-30	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-30V, V _{GS} =0V	--	--	-1	μA
	Zero Gate Voltage Drain Current(T _J =125°C)	V _{DS} =-30V, V _{GS} =0V	--	--	-100	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V, V _{DS} =0V	--	--	±100	nA
V _{GS(TH)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250μA	-1.3	-1.9	-2.4	V
R _{DS(ON)}	Drain-Source On-State Resistance ④	V _{GS} =-10V, I _D =-20A	--	10	13	mΩ
R _{DS(ON)}	Drain-Source On-State Resistance ④	V _{GS} =-4.5V, I _D =-16A	--	18	23	mΩ
Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise stated)						
C _{iss}	Input Capacitance	V _{DS} =-15V, V _{GS} =0V, f=1MHz	--	2555	--	pF
C _{oss}	Output Capacitance		--	290	--	pF
C _{rss}	Reverse Transfer Capacitance		--	200	--	pF
R _g	Gate Resistance	f=1MHz	--	3.1	--	Ω
Q _g	Total Gate Charge	V _{DS} =-15V, I _D =-20A, V _{GS} =-10V	--	44	--	nC
Q _{gs}	Gate-Source Charge		--	8	--	nC
Q _{gd}	Gate-Drain Charge		--	9.8	--	nC
Switching Characteristics						
t _{d(on)}	Turn-on Delay Time	V _{DD} =-15V, I _D =-20A, R _G =3.0Ω, V _{GS} =-10V	--	10.6	--	ns
t _r	Turn-on Rise Time		--	22	--	ns
t _{d(off)}	Turn-Off Delay Time		--	57	--	ns
t _f	Turn-Off Fall Time		--	32	--	ns
Source- Drain Diode Characteristics @ T_J = 25°C (unless otherwise stated)						
V _{SD}	Forward on voltage	I _{SD} =-20A, V _{GS} =0V	--	-0.9	-1.2	V
t _{rr}	Reverse Recovery Time	T _J =25°C, I _{sd} =-20A, V _{GS} =0V	--	40	--	ns
Q _{rr}	Reverse Recovery Charge	di/dt=-100A/μs	--	49	--	nC

NOTE:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = -11A, V_{GS} = -10V. Part not recommended for use above this value
- ③ The power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C.
- ④ Pulse width ≤ 300μs; duty cycles ≤ 2%.



-30V/-50A P-Channel Advanced Power MOSFET

Typical Characteristics

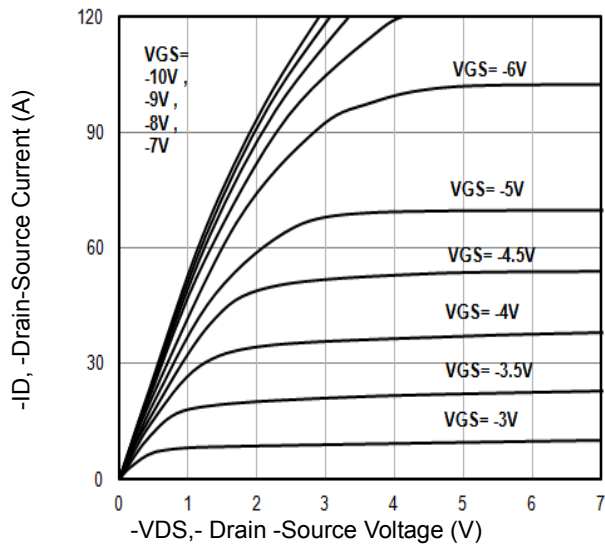


Fig1. Typical Output Characteristics

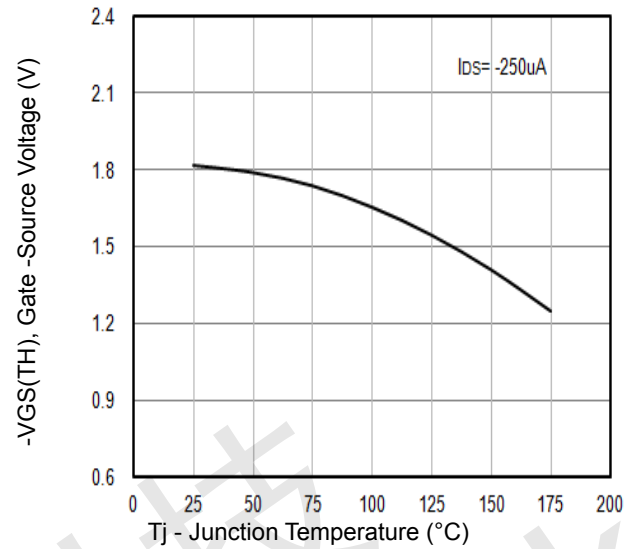


Fig2. $-V_{GS(TH)}$ Gate -Source Voltage Vs. T_j

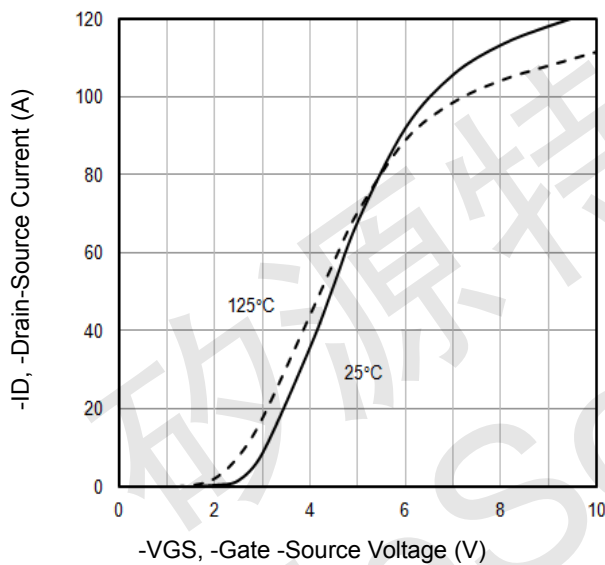


Fig3. Typical Transfer Characteristics

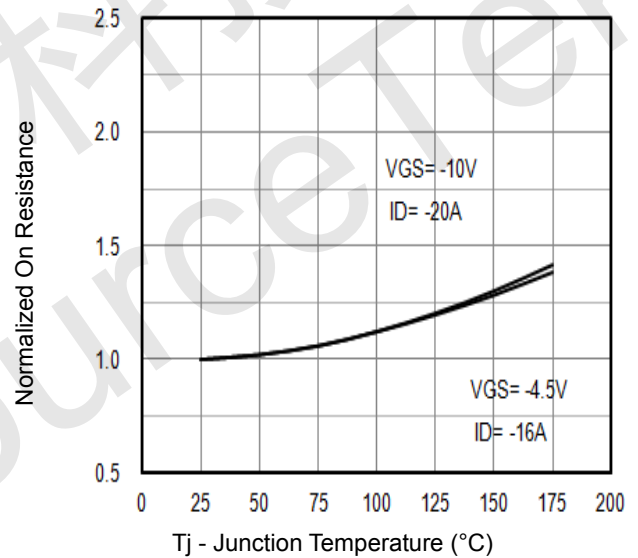


Fig4. Normalized On-Resistance Vs. T_j

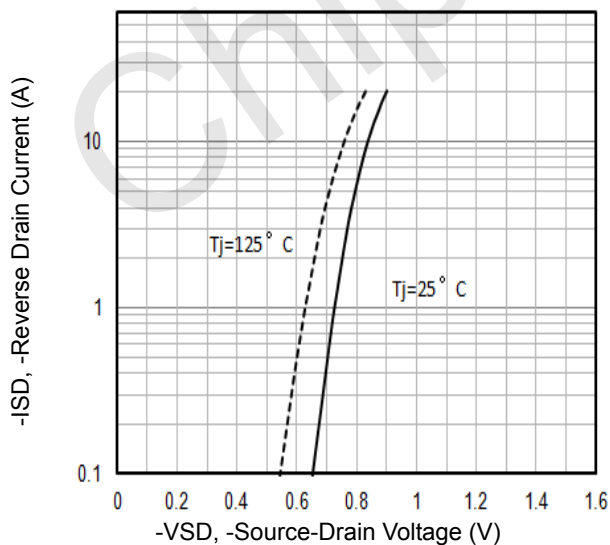


Fig5. Typical Source-Drain Diode Forward Voltage

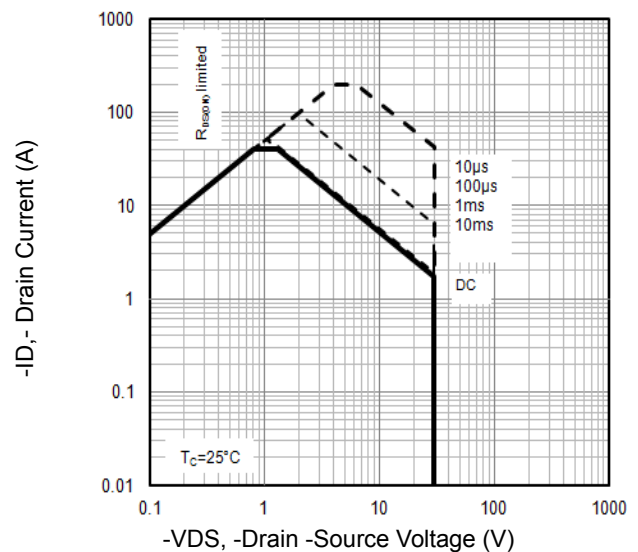


Fig6. Maximum Safe Operating Area



Typical Characteristics

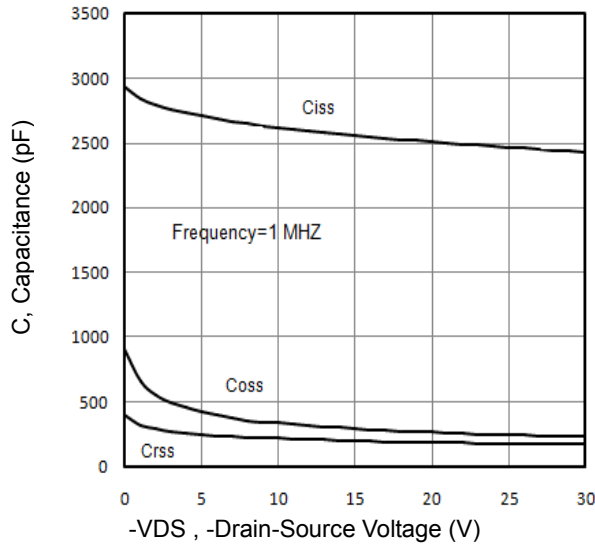


Fig7. Typical Capacitance Vs. Drain-Source Voltage

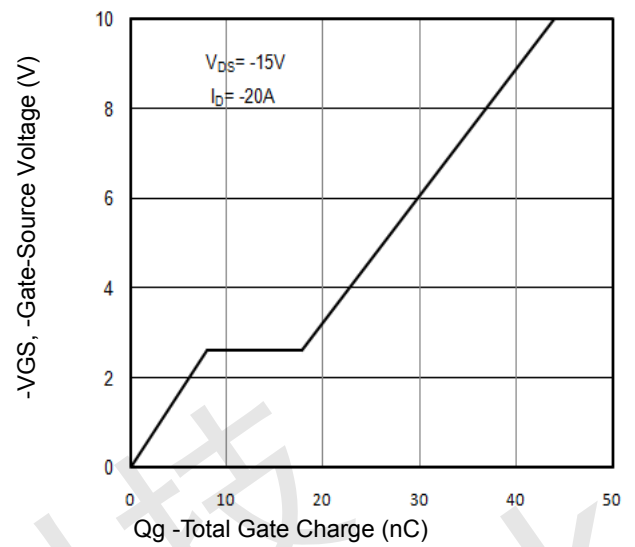


Fig8. Typical Gate Charge Vs. Gate-Source Voltage

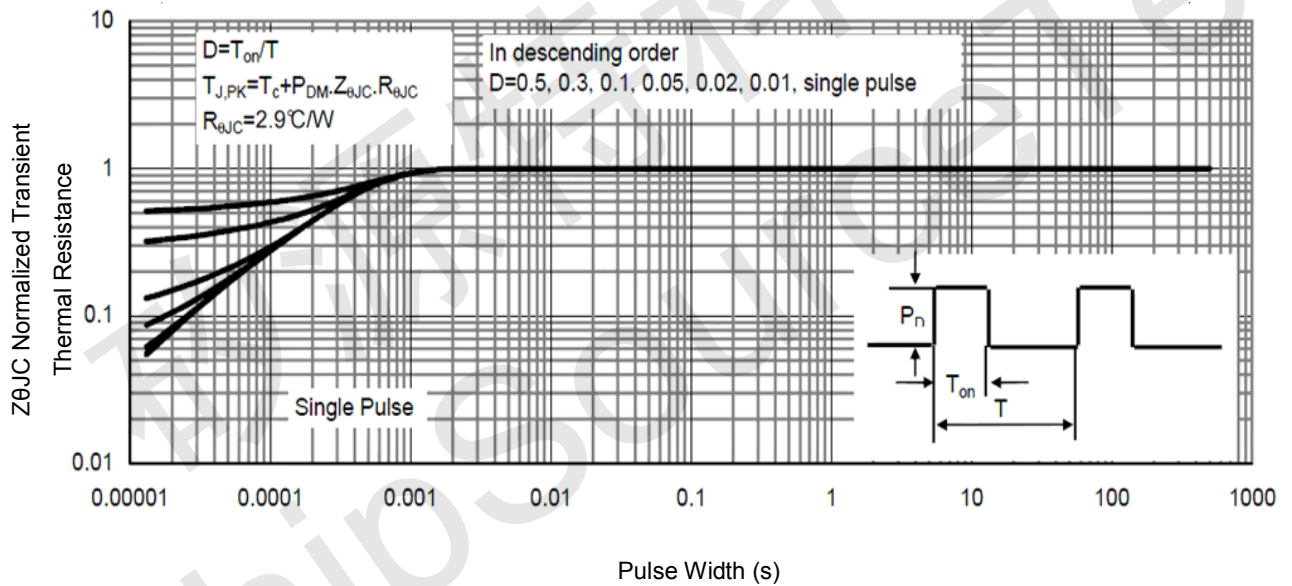


Fig9. Normalized Maximum Transient Thermal Impedance

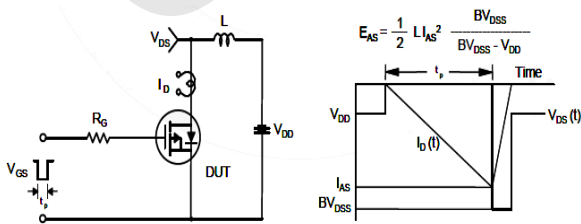


Fig10. Unclamped Inductive Test Circuit and Waveforms

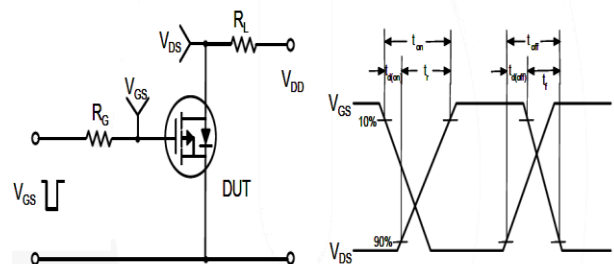
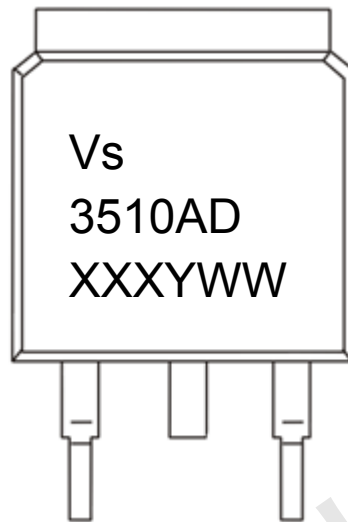


Fig11. Switching Time Test Circuit and waveforms



Marking Information

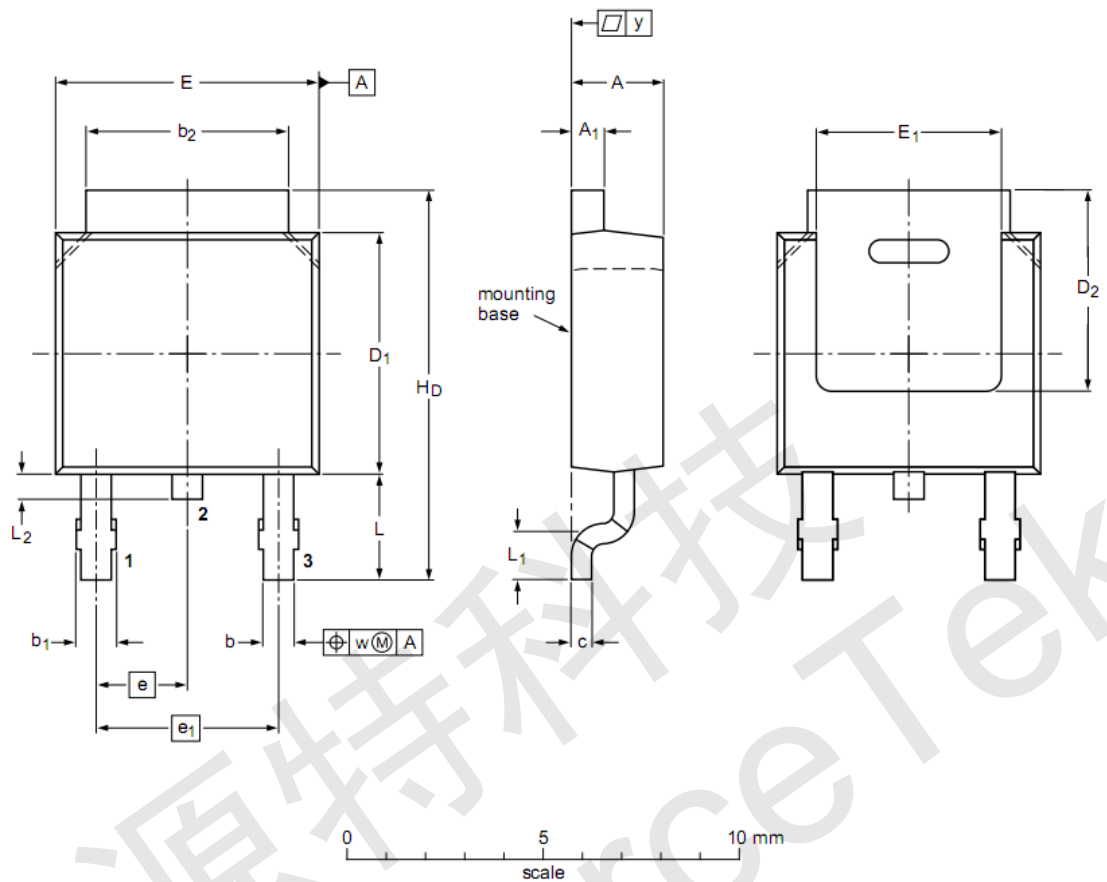


- 1st line: Company Code (Vs)
2nd line: Part Number (3510AD)
3rd line: Date code (XXXYWW)
XXX: Wafer Lot Number
Y: Year Code, e.g. E means 2017
WW: Week Code

矽源特科技
ChipSourceTek



TO-252 Package Outline Data



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	2.20	2.30	2.38
A ₁	0.46	0.50	0.63
b	0.64	0.76	0.89
b ₁	0.77	0.85	1.14
b ₂	5.00	5.33	5.46
c	0.458	0.508	0.558
D ₁	5.98	6.10	6.223
D ₂	5.21	--	--
E	6.40	6.60	6.731
E ₁	4.40	--	--
e	2.286 BSC		
e ₁	--	4.57	--
H _D	9.40	10.00	10.40
L	2.743 REF		
L ₁	1.40	1.52	1.77
L ₂	0.50	0.80	1.01
w	--	0.20	--
y	--	--	0.20

Notes:

1. Refer to JEDEC TO-252 variation AA
2. Dimension "E" does NOT include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.1524mm per side.
3. Dimension "D1" does NOT include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.1524mm per end.