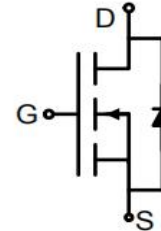




N-Channel Enhancement Mode Power MOSFET

Description

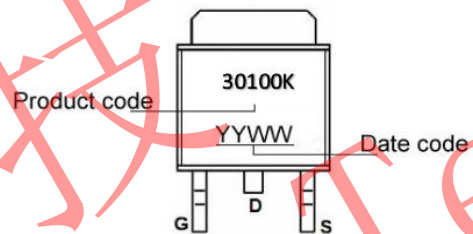
The MXD30N100 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$, with low gate charge. It can be used in a wide variety of applications.



General Features

- ◆ $V_{DS} = 30V$, $I_D = 100A$
- ◆ $R_{DS(ON)}$ (Typ.) $4m\Omega$ @ $V_{gs}=10V$
- ◆ $R_{DS(ON)}$ (Typ.) $7m\Omega$ @ $V_{gs}=4.5V$
- ◆ High density cell design for ultra low R_{dson}
- ◆ Fully characterized avalanche voltage and current
- ◆ Good stability and uniformity with high EAS
- ◆ Excellent package for good heat dissipation
- ◆ Special process technology for high ESD capability

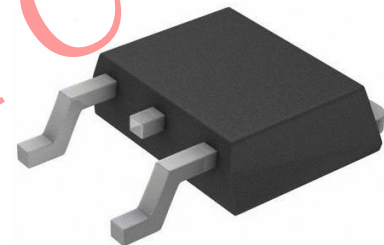
Schematic diagram



Marking and pin assignment

Application

- ◆ Power switching application
- ◆ Hard switched and high frequency circuits
- ◆ Uninterruptible power supply



TO-252-2L top view

Absolute Maximum Ratings (TA=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	100	A
Drain Current-Continuous($T_c=100^\circ C$)	$I_D(100^\circ C)$	70	A
Pulsed Drain Current	I_{DM}	400	A
Maximum Power Dissipation	P_D	110	W
Single pulse avalanche energy (Note 5)	EAS	350	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$



Electrical Characteristics (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	30	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1	1.6	3	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =30A	-	4.0	5.5	mΩ
		V _{GS} =4.5V, I _D =30A	-	7.0	8.5	mΩ
Forward Transconductance	g _{FS}	V _{DS} =10V, I _D =20A	50	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, F=1.0MHz		2100		PF
Output Capacitance	C _{oss}			390		PF
Reverse Transfer Capacitance	C _{rss}			270		PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =15V, I _D =60A V _{GS} =4.5V, R _{GEN} =1.8Ω	-	11	-	nS
Turn-on Rise Time	t _r		-	12	-	nS
Turn-Off Delay Time	t _{d(off)}		-	35	-	nS
Turn-Off Fall Time	t _f		-	30	-	nS
Total Gate Charge	Q _g	V _{DS} =15V, I _D =30A, V _{GS} =5V		50		nC
Gate-Source Charge	Q _{gs}			6		nC
Gate-Drain Charge	Q _{gd}			13		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V, I _S =20A	-	-	1.2	V
Diode Forward Current (Note 2)	I _S	-	-	-	100	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = 60A	-	56	-	nS
Reverse Recovery Charge	Q _{rr}	di/dt = 100A/μs(Note3)	-	110	-	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

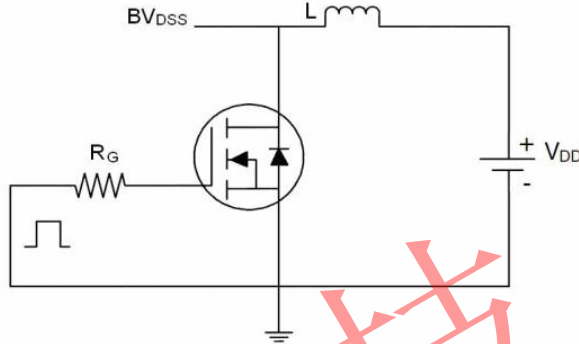
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS condition: T_J=25°C, V_{DD}=15V, V_G=10V, L=0.5mH, R_g=25Ω



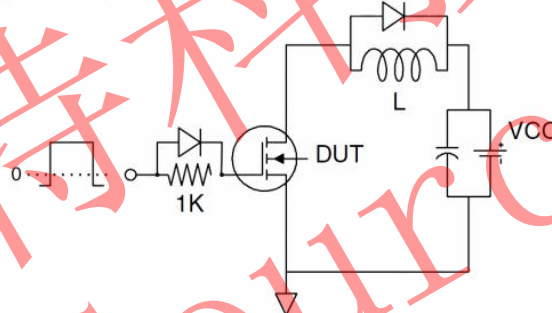
Typical Performance Characteristics

Test circuit

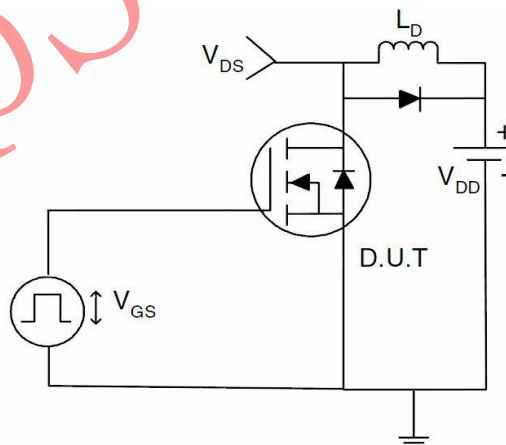
1) EAs test Circuits

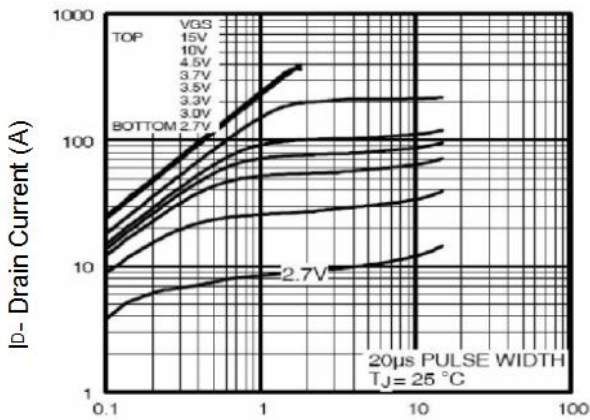


2) Gate charge test Circuit:



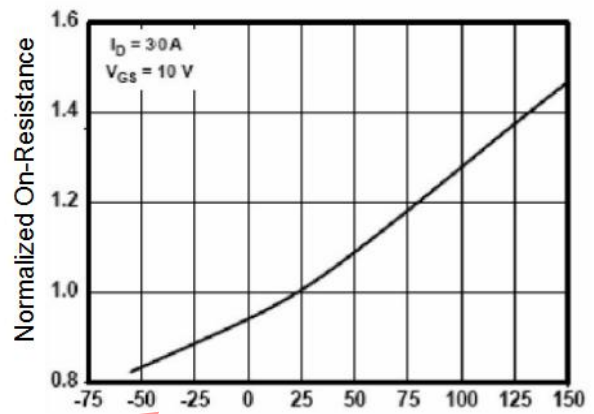
3) Switch Time Test Circuit:





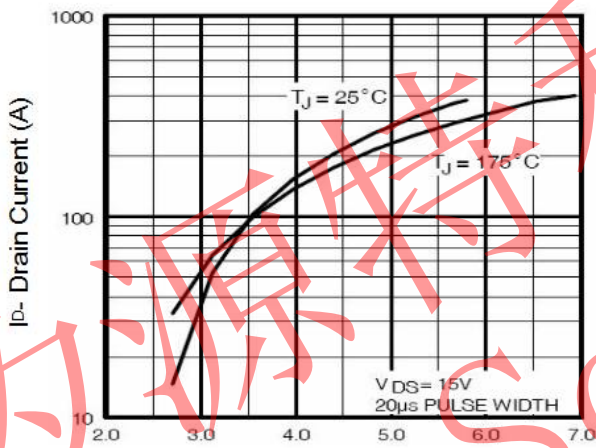
Vds Drain-Source Voltage (V)

Figure 1 Output Characteristics Figure



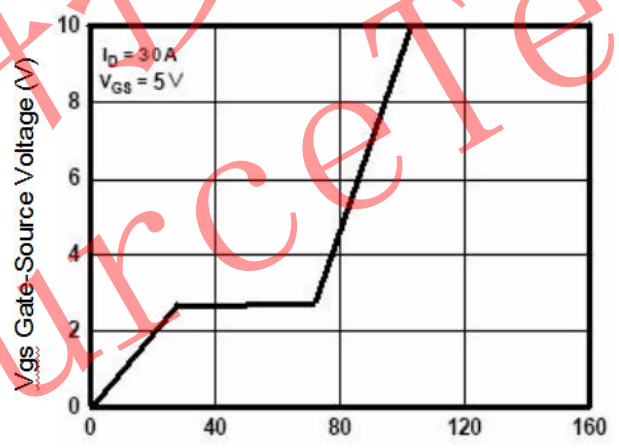
TJ Junction Temperature($^\circ\text{C}$)

4 Rdson-Junction Temperature



Vgs Gate-Source Voltage (V)

Figure 2 Transfer Characteristics



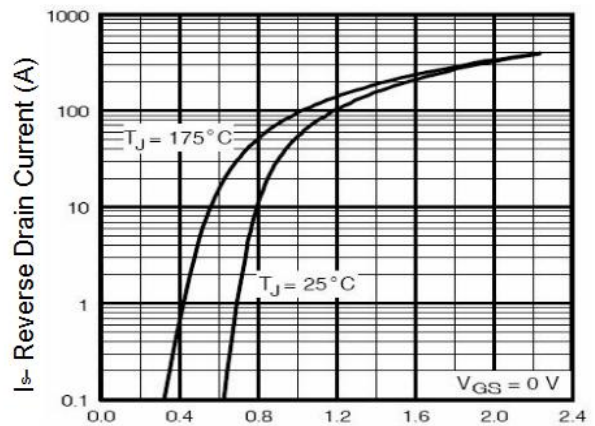
Qg Gate Charge (nC)

Figure 5 Gate Charge



ID- Drain Current (A)

Figure 3 Rdson- Drain Current



Vsd Source-Drain Voltage (V)

Figure 6 Source- Drain Diode Forward

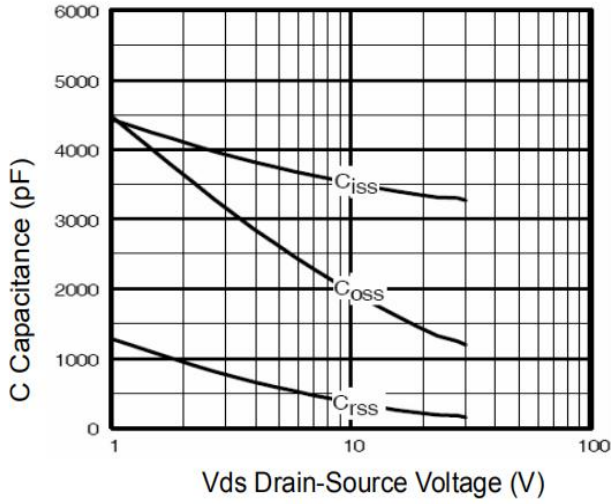


Figure 7 Capacitance vs Vds

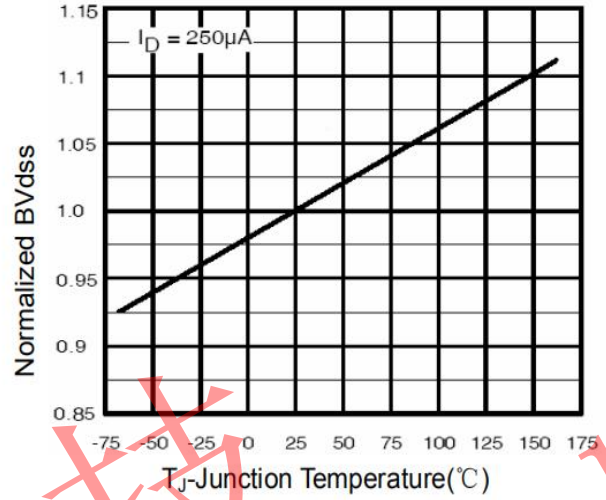


Figure 9 BV_{DSS} vs Junction Temperature

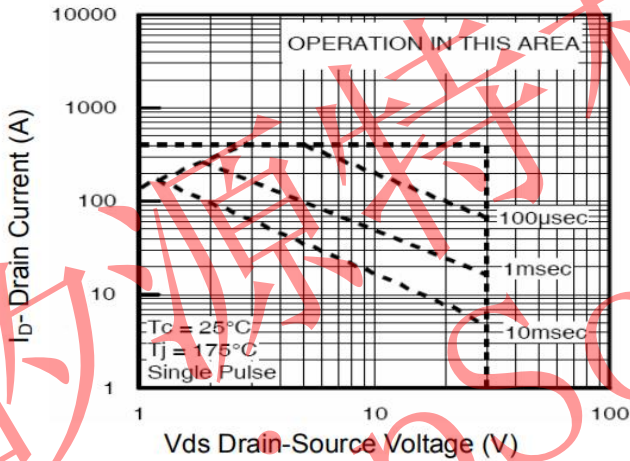


Figure 8 Safe Operation Area

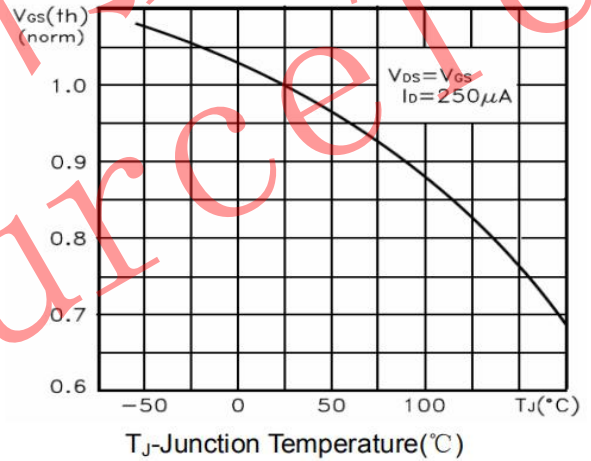


Figure 10 V_{GS(th)} vs Junction Temperature

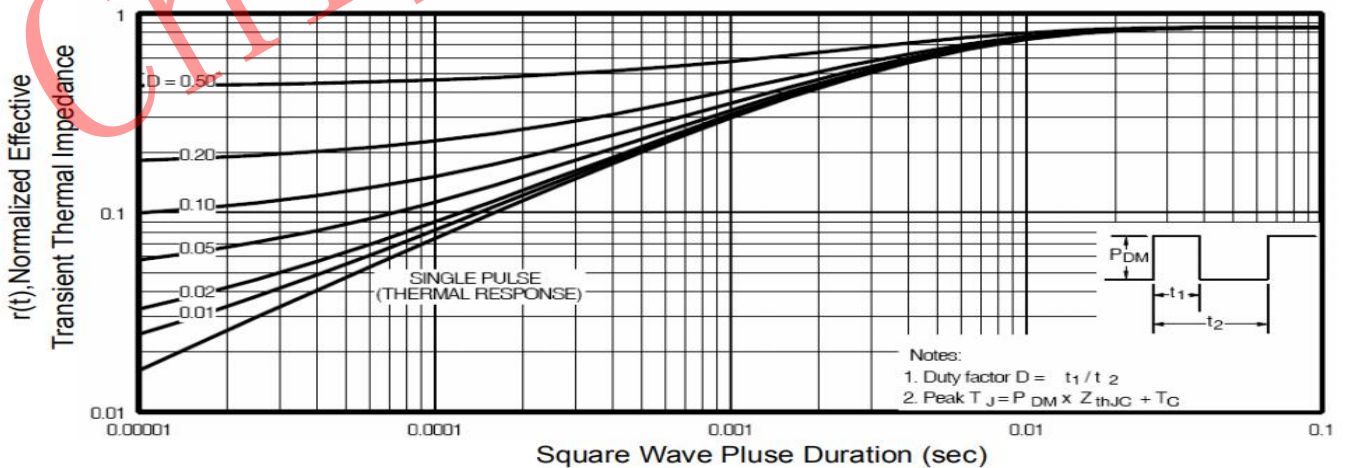
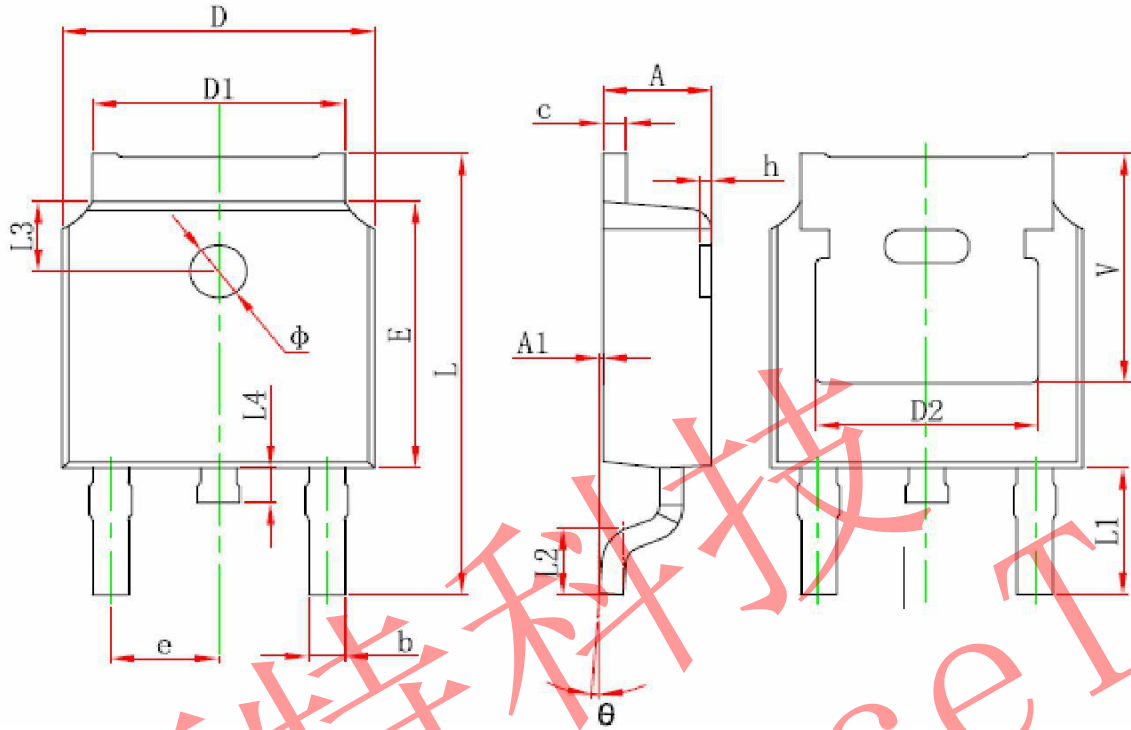


Figure 11 Normalized Maximum Transient Thermal Impedance



TO-252-2L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 REF.		0.190 REF.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 REF.		0.114 REF.	
L2	1.400	1.700	0.055	0.067
L3	1.600 REF.		0.063 REF.	
L4	0.600	1.000	0.024	0.039
φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 REF.		0.211 REF.	